CLAIMS

We Claim:

1. A method of making a semiconductor chip assembly, comprising:

providing a semiconductor chip, a conductive trace and a substrate, wherein the chip includes first and second opposing major surfaces and a conductive pad, the pad extends to the first surface of the chip, the substrate includes first and second opposing major surfaces, a conductive terminal and a dielectric base, the conductive terminal extends through the dielectric base to the first and second surfaces of the substrate, a cavity extends from the first surface of the substrate into the substrate, the first surfaces of the chip and the substrate face in a first direction, the second surfaces of the chip and the substrate face in a second direction, and the chip extends into the cavity; and then

electrically connecting the conductive terminal to the pad using the conductive trace.

2. The method of claim 1, including mechanically attaching the conductive trace to the chip using an adhesive before electrically connecting the conductive terminal to the pad.

3. The method of claim 2, including forming an opening through the adhesive that exposes the pad, and then forming a connection joint in the opening that contacts and electrically connects the conductive trace and the pad.

4. The method of claim 3, wherein the adhesive contacts and is sandwiched between the conductive trace and the pad, and the conductive trace and the pad are electrically isolated from one another after forming the opening and before forming the connection joint.

5. The method of claim 1, including mechanically attaching the conductive trace to the substrate using an adhesive before electrically connecting the conductive terminal to the pad.

6. The method of claim 5, including forming a via through the adhesive that exposes the conductive terminal, and then forming an interconnect in the via that contacts and electrically connects the conductive trace and the conductive terminal.

7. The method of claim 6, wherein the adhesive contacts and is sandwiched between the conductive trace and the conductive terminal, and the conductive trace and the conductive terminal are electrically isolated from one another after forming the via and before forming the interconnect.

8. The method of claim 1, including mechanically attaching the conductive trace to the chip and the substrate using an adhesive before electrically connecting the conductive terminal to the pad.

9. The method of claim 8, including forming an opening through the adhesive that exposes the pad, forming a via through the adhesive that exposes the conductive terminal, forming a connection joint in the opening that contacts and electrically connects the conductive trace and the pad, and forming an interconnect in the via that contacts and electrically connects the conductive trace and the conductive terminal.

10. The method of claim 9, wherein the adhesive contacts and is sandwiched between the conductive trace and the pad, and the conductive trace and the pad are electrically isolated from one another after forming the opening and before forming the connection joint, and the adhesive contacts and is sandwiched between the conductive trace and the conductive terminal, and the conductive trace and the conductive terminal are electrically isolated from one another after forming the via and before forming the interconnect.

11. The method of claim 1, including mechanically attaching the conductive trace to the chip, the conductive trace to the substrate, and the chip to the substrate using an adhesive before electrically connecting the conductive terminal to the pad.

12. The method of claim 11, including contacting the adhesive to the conductive trace, and then contacting the adhesive to the chip.

13. The method of claim 11, including contacting the adhesive to the conductive trace, and then contacting the adhesive to the substrate.

14. The method of claim 11, including contacting the adhesive to the chip, and then contacting the adhesive to the substrate.

15. The method of claim 11, including contacting the adhesive to the conductive trace, then contacting the adhesive to the chip, and then contacting the adhesive to the substrate.

16. The method of claim 11, including contacting the adhesive to the conductive trace, the chip and the substrate and then fully curing the adhesive.

17. The method of claim 11, including contacting the adhesive to the conductive trace and the chip, then partially curing a first portion of the adhesive that contacts the conductive trace and is proximate to the chip without partially curing a second portion of the adhesive that contacts the conductive trace and is not proximate to the chip, then contacting the adhesive to the substrate, and then partially curing the second portion of the adhesive that is proximate to the substrate.

18. The method of claim 11, including contacting the adhesive to the conductive trace and the chip, then partially curing a first portion of the adhesive that

contacts the conductive trace and is proximate to the chip without partially curing a second portion of the adhesive that contacts the conductive trace and is not proximate to the chip, then contacting the adhesive to the substrate, then partially curing the second portion of the adhesive that is proximate to the substrate, and then fully curing the first and second portions of the adhesive.

19. The method of claim 11, wherein the adhesive contacts and is sandwiched between the conductive trace and the pad, and the adhesive contacts and is sandwiched between the conductive trace and the conductive terminal.

20. The method of claim 11, wherein the adhesive is silicone, polyimide or epoxy.

21. The method of claim 1, including contacting a first adhesive to the conductive trace and the chip, contacting a second adhesive to the conductive trace, the substrate and the first adhesive, and mechanically attaching the conductive trace to the chip, the conductive trace to the substrate, and the chip to the substrate using an adhesive that includes the first and second adhesives before electrically connecting the conductive terminal to the pad.

22. The method of claim 21, including contacting the first adhesive to the conductive trace, and then contacting the first adhesive to the chip.

23. The method of claim 21, including contacting the second adhesive to the conductive trace and the first adhesive, and then contacting the second adhesive to the substrate.

24. The method of claim 21, including contacting the second adhesive to the substrate, and then contacting the second adhesive to the conductive trace and the first adhesive.

25. The method of claim 21, including contacting the first adhesive to the conductive trace, then contacting the first adhesive to the chip, and then contacting the second adhesive to the conductive trace, the substrate and the first adhesive.

26. The method of claim 21, including contacting the first adhesive to the conductive trace and the chip, then partially curing the first adhesive, then contacting the second adhesive to the conductive trace, the substrate and the first adhesive, and then partially curing the second adhesive.

27. The method of claim 21, including contacting the first adhesive to the conductive trace and the chip, then contacting the second adhesive to the conductive trace, the substrate and the first adhesive, and then fully curing the first and second adhesives.

28. The method of claim 21, including contacting the first adhesive to the conductive trace and the chip, then partially curing the first adhesive, then contacting the second adhesive to the conductive trace, the substrate and the first adhesive, then partially curing the second adhesive, and then fully curing the first and second adhesives.

29. The method of claim 21, wherein the adhesive contacts and is sandwiched between the conductive trace and the pad, and the adhesive contacts and is sandwiched between the conductive trace and the conductive terminal.

30. The method of claim 21, wherein the adhesive is silicone, polyimide or epoxy.

31. The method of claim 1, including contacting a first adhesive to the conductive trace, the substrate and the chip without depositing the first adhesive into

the cavity from the second surface of the substrate, contacting a second adhesive to the substrate and the first adhesive by depositing the second adhesive into the cavity from the second surface of the substrate, and mechanically attaching the conductive trace to the chip, the conductive trace to the substrate, and the chip to the substrate using an adhesive that includes the first and second adhesives before electrically connecting the conductive terminal to the pad.

32. The method of claim 31, including contacting the first adhesive to the conductive trace, and then contacting the first adhesive to the chip.

33. The method of claim 31, including contacting the first adhesive to the conductive trace, and then contacting the first adhesive to the substrate.

34. The method of claim 31, including contacting the first adhesive to the conductive trace, then contacting the first adhesive to the chip, and then contacting the first adhesive to the substrate.

35. The method of claim 31, including contacting a third first adhesive to the conductive trace and the chip, and then contacting a fourth adhesive to the conductive trace, the substrate and the third adhesive, wherein the first adhesive includes the third and fourth adhesives.

36. The method of claim 31, including contacting the first adhesive to the conductive trace and the chip, then partially curing the first adhesive, then contacting the second adhesive to the substrate and the first adhesive, and then partially curing the second adhesive.

37. The method of claim 31, including contacting the first adhesive to the conductive trace and the chip, then contacting the second adhesive to the substrate and the first adhesive, and then fully curing the first and second adhesives.

38. The method of claim 31, including contacting the first adhesive to the conductive trace and the chip, then partially curing the first adhesive, then contacting the second adhesive to the substrate and the first adhesive, then partially curing the second adhesive, and then fully curing the first and second adhesives.

39. The method of claim 31, wherein the adhesive contacts and is sandwiched between the conductive trace and the pad, and the adhesive contacts and is sandwiched between the conductive trace and the conductive terminal.

40. The method of claim 31, wherein the adhesive is silicone, polyimide or epoxy.

41. The method of claim 1, including mechanically attaching the conductive trace to the chip using an adhesive, then forming an opening in the adhesive that exposes the pad, and then forming a connection joint in the opening that contacts and electrically connects the conductive trace and the pad.

42. The method of claim 41, including contacting the adhesive to the conductive trace, then contacting the adhesive to the chip, then hardening the adhesive, and then forming the opening.

43. The method of claim 41, wherein the adhesive contacts and is sandwiched between the conductive trace and the pad after mechanically attaching the conductive trace to the chip and before forming the opening.

44. The method of claim 41, wherein the adhesive contacts and is sandwiched between the conductive trace and the pad after forming the opening and before forming the connection joint.

45. The method of claim 41, wherein the adhesive contacts and is sandwiched between the conductive trace and the pad after forming the connection joint.

46. The method of claim 41, wherein forming the opening includes applying a laser that ablates the adhesive.

47. The method of claim 41, wherein forming the opening includes applying a plasma that etches the adhesive.

48. The method of claim 41, wherein forming the opening exposes a peripheral sidewall of the conductive trace.

49. The method of claim 41, wherein forming the opening exposes opposing peripheral sidewalls of the conductive trace.

50. The method of claim 41, wherein the adhesive is silicone, polyimide or epoxy, and the connection joint is an electroplated metal, an electrolessly plated metal, a ball bond, a weld, solder or conductive adhesive.

51. The method of claim 1, including mechanically attaching the conductive trace to the substrate using an adhesive, then forming a via in the adhesive that exposes the conductive terminal, and then forming an interconnect in the via that contacts and electrically connects the conductive trace and the conductive terminal.

52. The method of claim 51, including contacting the adhesive to the conductive trace, then contacting the adhesive to the substrate, then hardening the adhesive, and then forming the via.

53. The method of claim 51, wherein the adhesive contacts and is sandwiched between the conductive trace and the conductive terminal after mechanically attaching the conductive trace to the substrate and before forming the via.

54. The method of claim 51, wherein the adhesive contacts and is sandwiched between the conductive trace and the conductive terminal after forming the via and before forming the interconnect.

55. The method of claim 51, wherein the adhesive contacts and is sandwiched between the conductive trace and the conductive terminal after forming the interconnect.

56. The method of claim 51, wherein forming the via includes applying a laser that ablates the adhesive.

57. The method of claim 51, wherein forming the via includes applying a plasma that etches the adhesive.

58. The method of claim 51, wherein forming the via exposes a peripheral sidewall of the conductive trace.

59. The method of claim 51, wherein forming the via exposes opposing peripheral sidewalls of the conductive trace.

60. The method of claim 51, wherein the adhesive is silicone, polyimide or epoxy, and the interconnect is an electroplated metal, an electrolessly plated metal, a ball bond, a weld, solder or conductive adhesive.

61. The method of claim 1, including:

disposing an adhesive between the conductive trace and the pad and between the conductive trace and the conductive terminal;

forming an opening that extends through the adhesive and exposes the pad;

forming a connection joint in the opening that electrically connects the conductive trace and the pad;

forming a via that extends through the adhesive and exposes the conductive terminal; and

forming an interconnect in the via that electrically connects the conductive trace and the conductive terminal.

62. The method of claim 61, wherein the conductive trace extends within and outside a periphery of the chip.

63. The method of claim 62, wherein the opening and the connection joint are disposed within the periphery of the chip.

64. The method of claim 62, wherein the via and the interconnect are disposed outside the periphery of the chip.

65. The method of claim 62, wherein the opening and the connection joint are disposed within the periphery of the chip, and the via and the interconnect are disposed outside the periphery of the chip.

66. The method of claim 61, wherein forming the opening includes applying a laser that ablates the adhesive, and forming the via includes applying a laser that ablates the adhesive.

67. The method of claim 61, wherein forming the connection joint includes plating a metal on the conductive trace and the pad, and forming the interconnect includes plating a metal on the conductive trace and the conductive terminal.

68. The method of claim 61, including sequentially forming the opening and the via.

69. The method of claim 61, including sequentially forming the connection joint and the interconnect.

70. The method of claim 61, including simultaneously forming the connection joint and the interconnect.

71. The method of claim 1, including:

disposing an adhesive between the conductive trace and the pad and between the conductive trace and the conductive terminal; then

forming (i) an opening that extends through the adhesive and exposes the pad and (ii) a via that extends through the adhesive and exposes the conductive terminal; and then

forming (i) a connection joint in the opening that contacts and electrically connects the conductive trace and the pad and (ii) an interconnect in the via that contacts and electrically connects the conductive trace and the conductive terminal.

72. The method of claim 71, wherein the conductive trace extends within and outside a periphery of the chip.

73. The method of claim 72, wherein the opening and the connection joint are disposed within the periphery of the chip.

74. The method of claim 72, wherein the via and the interconnect are disposed outside the periphery of the chip.

75. The method of claim 72, wherein the opening and the connection joint are disposed within the periphery of the chip, and the via and the interconnect are disposed outside the periphery of the chip.

76. The method of claim 71, wherein forming the opening includes applying a laser that ablates the adhesive, and forming the via includes applying a laser that ablates the adhesive.

77. The method of claim 71, wherein forming the connection joint includes plating a metal on the conductive trace and the pad, and forming the interconnect includes plating a metal on the conductive trace and the conductive terminal.

78. The method of claim 71, including sequentially forming the opening and the via.

79. The method of claim 71, including sequentially forming the connection joint and the interconnect.

80. The method of claim 71, including simultaneously forming the connection joint and the interconnect.

81. The method of claim 1, including:

disposing an adhesive between the conductive trace and the pad and between the conductive trace and the conductive terminal; then

forming (i) an opening that extends through the adhesive and exposes the pad and (ii) a connection joint in the opening that contacts and electrically connects the conductive trace and the pad; and then

forming (i) a via that extends through the adhesive and exposes the conductive terminal and (ii) an interconnect in the via that contacts and electrically connects the conductive trace and the conductive terminal.

82. The method of claim 81, wherein the conductive trace extends within and outside a periphery of the chip.

83. The method of claim 82, wherein the opening and the connection joint are disposed within the periphery of the chip.

84. The method of claim 82, wherein the via and the interconnect are disposed outside the periphery of the chip.

85. The method of claim 82, wherein the opening and the connection joint are disposed within the periphery of the chip, and the via and the interconnect are disposed outside the periphery of the chip.

86. The method of claim 81, wherein forming the opening includes applying a laser that ablates the adhesive, and forming the via includes applying a laser that ablates the adhesive.

87. The method of claim 81, wherein forming the connection joint includes plating a metal on the conductive trace and the pad.

88. The method of claim 81, wherein forming the interconnect includes depositing solder or conductive adhesive on the conductive trace and the conductive terminal.

89. The method of claim 81, wherein forming the connection joint includes plating a metal on the conductive trace and the pad, and forming the interconnect includes depositing solder or conductive adhesive on the conductive trace and the conductive terminal.

90. The method of claim 81, wherein the connection joint is copper or nickel and the interconnect is solder or conductive adhesive.

91. The method of claim 1, including:

disposing an adhesive between the conductive trace and the pad; then

forming (i) an opening that extends through the adhesive between the conductive trace and the pad and exposes the pad and (ii) a connection joint in the opening that contacts and electrically connects the conductive trace and the pad; then

disposing an adhesive between the conductive trace and the conductive terminal; and then

forming (i) a via that extends through the adhesive between the conductive trace and the conductive terminal and exposes the conductive terminal and (ii) an interconnect in the via that contacts and electrically connects the conductive trace and the conductive terminal.

92. The method of claim 91, wherein the conductive trace extends within and outside a periphery of the chip.

93. The method of claim 92, wherein the opening and the connection joint are disposed within the periphery of the chip.

94. The method of claim 92, wherein the via and the interconnect are disposed outside the periphery of the chip.

95. The method of claim 92, wherein the opening and the connection joint are disposed within the periphery of the chip, and the via and the interconnect are disposed outside the periphery of the chip.

96. The method of claim 91, wherein forming the opening includes applying a laser that ablates the adhesive between the conductive trace and the pad, and forming

the via includes applying a laser that ablates the adhesive between the conductive trace and the conductive terminal.

97. The method of claim 91, wherein forming the connection joint includes plating a metal on the conductive trace and the pad.

98. The method of claim 91, wherein forming the interconnect includes depositing solder or conductive adhesive on the conductive trace and the conductive terminal.

99. The method of claim 91, wherein forming the connection joint includes plating a metal on the conductive trace and the pad, and forming the interconnect includes depositing solder or conductive adhesive on the conductive trace and the conductive terminal.

100. The method of claim 91, wherein the connection joint is copper or nickel and the interconnect is solder or conductive adhesive.

101. The method of claim 1, including simultaneously forming (i) a connection joint that contacts and electrically connects the conductive trace and the pad and (ii) an interconnect that contacts and electrically connects the conductive trace and the conductive terminal.

102. The method of claim 101, including simultaneously forming the connection joint and the interconnect during a plating operation.

103. The method of claim 102, wherein the plating operation includes an electroplating operation.

104. The method of claim 102, wherein the plating operation includes an electroless plating operation.

105. The method of claim 101, wherein the conductive trace extends within and outside a periphery of the chip.

106. The method of claim 105, wherein the connection joint is disposed within the periphery of the chip.

107. The method of claim 105, wherein the interconnect is disposed outside the periphery of the chip.

108. The method of claim 105, wherein the connection joint is disposed within the periphery of the chip, and the interconnect is disposed outside the periphery of the chip.

109. The method of claim 105, wherein the conductive terminal is disposed outside the cavity.

110. The method of claim 101, wherein the connection joint and the interconnect are copper or nickel.

111. The method of claim 1, including forming (i) a connection joint that contacts and electrically connects the conductive trace and the pad and then (ii) an interconnect that contacts and electrically connects the conductive trace and the conductive terminal.

112. The method of claim 111, including forming the connection joint before mechanically attaching the conductive trace to the substrate.

113. The method of claim 111, including forming the connection joint after mechanically attaching the conductive trace to the substrate.

114. The method of claim 111, including forming the interconnect after mechanically attaching the conductive trace to the substrate.

115. The method of claim 111, wherein the conductive trace extends within and outside a periphery of the chip.

116. The method of claim 115, wherein the connection joint is disposed within the periphery of the chip.

117. The method of claim 115, wherein the interconnect is disposed outside the periphery of the chip.

118. The method of claim 115, wherein the connection joint is disposed within the periphery of the chip, and the interconnect is disposed outside the periphery of the chip.

119. The method of claim 115, wherein the conductive terminal is disposed outside the cavity.

120. The method of claim 111, wherein the connection joint is a plated metal, and the interconnect is solder or conductive adhesive.

121. The method of claim 1, including mechanically attaching the conductive trace to the chip such that the conductive trace overlaps the pad, and then forming a connection joint that contacts and electrically connects the conductive trace and the pad.

122. The method of claim 121, wherein the conductive trace is essentially flat and parallel to the first surface of the chip.

123. The method of claim 121, wherein the conductive trace overlaps only one peripheral edge of the pad after mechanically attaching the conductive trace to the chip.

124. The method of claim 121, wherein the conductive trace overlaps only two peripheral edges of the pad, and the two peripheral edges are opposite one another, after mechanically attaching the conductive trace to the chip.

125. The method of claim 121, wherein the conductive trace overlaps only three peripheral edges of the pad, and two of the three peripheral edges are opposite one another, after mechanically attaching the conductive trace to the chip.

126. The method of claim 121, wherein the connection joint contacts a surface of the conductive trace that is disposed above and overlaps and faces away from the pad.

127. The method of claim 121, wherein the connection joint contacts a peripheral sidewall of the conductive trace that is disposed above and overlaps and is orthogonal to the pad.

128. The method of claim 121, wherein the connection joint contacts opposing peripheral sidewalls of the conductive trace that are disposed above and overlap and are orthogonal to the pad.

129. The method of claim 121, wherein the connection joint is a plated metal.

130. The method of claim 121, wherein the connection joint is devoid of wire bonds and TAB leads.

131. The method of claim 1, including:

mechanically attaching a connection joint to the chip; then

aligning the conductive trace with the chip such that the conductive trace overlaps the pad; and then

simultaneously mechanically attaching the conductive trace to the chip with a solid mechanical bond and reshaping the connection joint, wherein the connection joint contacts and electrically connects the conductive trace and the pad after the reshaping.

132. The method of claim 131, wherein the conductive trace is essentially flat and parallel to the first surface of the chip.

133. The method of claim 131, wherein the conductive trace overlaps only one peripheral edge of the pad after mechanically attaching the conductive trace to the chip.

134. The method of claim 131, wherein the conductive trace overlaps only two peripheral edges of the pad, and the two peripheral edges are opposite one another, after mechanically attaching the conductive trace to the chip.

135. The method of claim 131, wherein the conductive trace overlaps only three peripheral edges of the pad, and two of the three peripheral edges are opposite one another, after mechanically attaching the conductive trace to the chip.

136. The method of claim 131, wherein the connection joint contacts a surface of the conductive trace that is disposed above and overlaps and faces towards the pad.

137. The method of claim 131, wherein the connection joint contacts a peripheral sidewall of the conductive trace that is disposed above and overlaps and is orthogonal to the pad.

138. The method of claim 131, wherein the connection joint contacts opposing peripheral sidewalls of the conductive trace that are disposed above and overlap and are orthogonal to the pad.

139. The method of claim 131, wherein the connection joint is solder or conductive adhesive.

140. The method of claim 131, wherein the connection joint is devoid of wire bonds and TAB leads.

141. The method of claim 1, including mechanically attaching the conductive trace to the substrate such that the conductive trace overlaps the conductive terminal, and then forming an interconnect that contacts and electrically connects the conductive trace and the conductive terminal.

142. The method of claim 141, wherein the conductive trace is essentially flat and parallel to the first surface of the substrate.

143. The method of claim 141, wherein the conductive trace overlaps only one peripheral edge of the conductive terminal after mechanically attaching the conductive trace to the substrate.

144. The method of claim 141, wherein the conductive trace overlaps only two peripheral edges of the conductive terminal, and the two peripheral edges are opposite one another, after mechanically attaching the conductive trace to the substrate.

145. The method of claim 141, wherein the conductive trace overlaps only three peripheral edges of the conductive terminal, and two of the three peripheral edges are opposite one another, after mechanically attaching the conductive trace to the substrate.

146. The method of claim 141, wherein the interconnect contacts a surface of the conductive trace that is disposed above and overlaps and faces away from the conductive terminal.

147. The method of claim 141, wherein the interconnect contacts a peripheral sidewall of the conductive trace that is disposed above and overlaps and is orthogonal to the conductive terminal.

148. The method of claim 141, wherein the interconnect contacts opposing peripheral sidewalls of the conductive trace that are disposed above and overlap and are orthogonal to the conductive terminal.

149. The method of claim 141, wherein the interconnect is a plated metal.

150. The method of claim 141, wherein the interconnect is devoid of wire bonds and TAB leads.

151. The method of claim 1, including:

mechanically attaching an interconnect to the substrate; then

aligning the conductive trace with the substrate such that the conductive trace overlaps the conductive terminal; and then

simultaneously mechanically attaching the conductive trace to the substrate with a solid mechanical bond and reshaping the interconnect, wherein the interconnect contacts and electrically connects the conductive trace and the conductive terminal after the reshaping.

152. The method of claim 151, wherein the conductive trace is essentially flat and parallel to the first surface of the substrate.

153. The method of claim 151, wherein the conductive trace overlaps only one peripheral edge of the conductive terminal after mechanically attaching the conductive trace to the substrate.

154. The method of claim 151, wherein the conductive trace overlaps only two peripheral edges of the conductive terminal, and the two peripheral edges are opposite one another, after mechanically attaching the conductive trace to the substrate.

155. The method of claim 151, wherein the conductive trace overlaps only three peripheral edges of the conductive terminal, and two of the three peripheral edges are opposite one another, after mechanically attaching the conductive trace to the substrate.

156. The method of claim 151, wherein the interconnect contacts a surface of the conductive trace that is disposed above and overlaps and faces towards the conductive terminal.

157. The method of claim 151, wherein the interconnect contacts a peripheral sidewall of the conductive trace that is disposed above and overlaps and is orthogonal to the conductive terminal.

158. The method of claim 151, wherein the interconnect contacts opposing peripheral sidewalls of the conductive trace that are disposed above and overlap and are orthogonal to the conductive terminal.

159. The method of claim 151, wherein the interconnect is solder or conductive adhesive.

160. The method of claim 151, wherein the interconnect is devoid of wire bonds and TAB leads.

161. The method of claim 1, including mechanically attaching the chip to the substrate without applying pressure to the second surface of the chip.

162. The method of claim 161, wherein the first surface of the chip is disposed outside the cavity.

163. The method of claim 161, wherein the first surface of the chip is essentially coplanar with the conductive terminal at the first surface of the substrate.

164. The method of claim 161, wherein the second surface of the chip is disposed within the cavity.

165. The method of claim 161, wherein the second surface of the chip is spaced from the substrate by an open gap.

166. The method of claim 161, wherein the second surface of the chip is exposed.

167. The method of claim 161, wherein the cavity has a generally rectangular shape bounded by inner sidewalls of the dielectric base.

168. The method of claim 161, wherein the cavity is spaced from the conductive terminal.

169. The method of claim 161, wherein the cavity extends into but not through the substrate.

170. The method of claim 161, wherein the cavity extends through the substrate.

171. The method of claim 1, including mechanically attaching the chip to the substrate such that an adhesive is disposed between the conductive trace and the pad, the adhesive is disposed between the conductive trace and the conductive terminal, the adhesive extends into the cavity, and the cavity is sealed at the first surface of the substrate.

172. The method of claim 171, wherein the first surface of the chip is disposed outside the cavity.

173. The method of claim 171, wherein the first surface of the chip is essentially coplanar with the conductive terminal at the first surface of the substrate.

174. The method of claim 171, wherein the second surface of the chip is disposed within the cavity.

175. The method of claim 171, wherein the second surface of the chip is spaced from the substrate by an open gap.

176. The method of claim 171, wherein the second surface of the chip is exposed.

177. The method of claim 171, wherein the cavity has a generally rectangular shape bounded by inner sidewalls of the dielectric base.

178. The method of claim 171, wherein the cavity is spaced from the conductive terminal.

179. The method of claim 171, wherein the cavity extends into but not through the substrate.

180. The method of claim 171, wherein the cavity extends through the substrate.

181. The method of claim 1, including mechanically attaching the conductive trace to the chip and the substrate such that the conductive trace is proximate to and electrically isolated from the conductive terminal and the pad.

182. The method of claim 181, wherein the first surface of the chip is disposed outside the cavity.

183. The method of claim 181, wherein the first surface of the chip is essentially coplanar with the conductive terminal at the first surface of the substrate.

184. The method of claim 181, wherein the second surface of the chip is disposed within the cavity.

185. The method of claim 181, wherein the second surface of the chip is spaced from the substrate by an open gap.

186. The method of claim 181, wherein the second surface of the chip is exposed.

187. The method of claim 181, wherein the cavity has a generally rectangular shape bounded by inner sidewalls of the dielectric base.

188. The method of claim 181, wherein the cavity is spaced from the conductive terminal.

189. The method of claim 181, wherein the cavity extends into but not through the substrate.

190. The method of claim 181, wherein the cavity extends through the substrate.

191. The method of claim 1, including mechanically attaching the conductive trace to the chip and the substrate such that the conductive trace includes first and second distal ends, the conductive terminal includes first and second contact terminals at the first and second surfaces, respectively, of the substrate, the first end is proximate to and spaced from the pad, and the second end is proximate to and spaced from the first contact terminal.

192. The method of claim 191, wherein the conductive trace has a first pitch at the first end with other conductive traces that are spaced from the chip and the substrate, the conductive trace has a second pitch at the second end with the other conductive traces, and the first pitch is less than the second pitch.

193. The method of claim 191, wherein the conductive terminal has a third pitch at the first contact terminal with other conductive terminals that extend through the dielectric base, the conductive terminal has a fourth pitch at the second contact terminal with the other conductive terminals, and the third pitch is less than the fourth pitch.

194. The method of claim 191, wherein:

the conductive trace has a first pitch at the first end with other conductive traces that are spaced from the chip and the substrate, the conductive trace has a second pitch at the second end with the other conductive traces, and the first pitch is less than the second pitch; and

the conductive terminal has a third pitch at the first contact terminal with other conductive terminals that extend through the dielectric base, the conductive terminal has a fourth pitch at the second contact terminal with the other conductive terminals, and the third pitch is less than the fourth pitch.

195. The method of claim 194, wherein the second and third pitches are essentialiy identical.

196. The method of claim 194, wherein the conductive trace provides horizontal routing within and outside a periphery of the chip.

197. The method of claim 196, wherein the conductive trace does not provide vertical routing.

198. The method of claim 194, wherein the conductive terminal provides horizontal and vertical routing outside a periphery of the chip.

199. The method of claim 198, wherein the conductive terminal provides horizontal routing at the first surface of the substrate and vertical routing between the first and second surfaces of the substrate.

200. The method of claim 194, wherein the conductive trace provides horizontal routing within and outside a periphery of the chip and does not provide vertical routing, and the conductive terminal provides horizontal and vertical routing outside the periphery of the chip.

201. The method of claim 1, including electrically connecting the conductive terminal to the pad such that the conductive trace provides fine-pitch fan-out routing for the pad and the conductive terminal provides coarse-pitch fan-out routing for the pad.

202. The method of claim 201, wherein the conductive trace has a larger pitch proximate to the conductive terminal than proximate to the pad.

203. The method of claim 201, wherein the conductive terminal has a larger pitch at the second surface of the substrate than proximate to the conductive trace.

204. The method of claim 201, wherein:

the conductive trace has a larger pitch proximate to the conductive terminal than proximate to the pad; and

the conductive terminal has a larger pitch at the second surface of the substrate than proximate to the conductive trace.

205. The method of claim 204, wherein the conductive trace and the conductive terminal have essentially identical pitches where they are proximate to one another.

206. The method of claim 204, wherein the conductive trace provides horizontal routing within and outside a periphery of the chip.

207. The method of claim 206, wherein the conductive trace does not provide vertical routing.

208. The method of claim 204, wherein the conductive terminal provides horizontal and vertical routing outside a periphery of the chip.

209. The method of claim 208, wherein the conductive terminal provides horizontal routing at the first surface of the substrate and provides vertical routing between the first and second surfaces of the substrate.

210. The method of claim 204, wherein the conductive trace provides horizontal routing within and outside a periphery of the chip and does not provide vertical routing, and the conductive terminal provides horizontal and vertical routing outside the periphery of the chip.

211. The method of claim 1, including electrically connecting the conductive terminal to the pad such that the conductive trace provides horizontal routing for the pad and the conductive terminal provides horizontal and vertical routing for the pad.

212. The method of claim 211, wherein the conductive trace provides horizontal routing within and outside a periphery of the chip.

213. The method of claim 211, wherein the conductive trace does not provide vertical routing.

214. The method of claim 211, wherein the conductive terminal provides horizontal routing outside a periphery of the chip.

215. The method of claim 211, wherein the conductive terminal provides horizontal routing at the first surface of the substrate.

216. The method of claim 211, wherein the conductive terminal provides vertical routing between the first and second surfaces of the substrate.

217. The method of claim 211, wherein the conductive trace provides horizontal routing within and outside a periphery of the chip, and the conductive terminal provides horizontal and vertical routing outside the periphery of the chip.

218. The method of claim 217, wherein the conductive trace does not provide vertical routing.

219. The method of claim 218, wherein the conductive terminal provides horizontal routing at the first surface of the substrate and vertical routing between the first and second surfaces of the substrate.

220. The method of claim 219, wherein a connection joint provides vertical routing between the conductive trace and the pad, and an interconnect provides vertical routing between the conductive trace and the conductive terminal.

221. The method of claim 1, including:

attaching the conductive trace to a metal base; then

mechanically attaching the conductive trace to the chip and the substrate; and then

etching the metal base, thereby exposing the conductive trace.

222. The method of claim 221, wherein attaching the conductive trace to the metal base includes electroplating the conductive trace on the metal base.

223. The method of claim 221, wherein mechanically attaching the conductive trace to the substrate includes contacting an adhesive to the conductive trace, the substrate and the metal base.

224. The method of claim 221, wherein mechanically attaching the conductive trace to the substrate includes soldering the conductive trace to the substrate.

225. The method of claim 221, wherein etching the metal base includes applying a wet chemical etch that is selective of the metal base with respect to the conductive trace.

226. The method of claim 221, wherein etching the metal base removes all of the metal base that overlaps the conductive trace.

227. The method of claim 221, wherein etching the metal base removes all of the metal base that overlaps the chip.

228. The method of claim 221, wherein etching the metal base removes all of the metal base that overlaps the substrate.

229. The method of claim 221, wherein etching the metal base removes all of the metal base that overlaps the conductive trace, the chip and the substrate.

230. The method of claim 221, wherein etching the metal base removes the metal base.

231. The method of claim 1, including:

attaching the conductive trace and other conductive traces to a metal base, thereby electrically connecting the conductive trace to the other conductive traces; then

mechanically attaching the conductive trace and the other conductive traces to the chip and the substrate; and then

etching the metal base, thereby electrically isolating the conductive trace from the other conductive traces.

232. The method of claim 231, wherein attaching the conductive trace and the other conductive traces to the metal base includes electroplating the conductive trace and the other conductive traces on the metal base.

233. The method of claim 231, wherein mechanically attaching the conductive trace and the other conductive traces to the substrate includes contacting an adhesive to the conductive trace, the other conductive trace, the substrate and the metal base.

234. The method of claim 231, wherein mechanically attaching the conductive trace and the other conductive traces to the substrate includes soldering the conductive trace and the other conductive traces to the substrate.

235. The method of claim 231, wherein etching the metal base includes applying a wet chemical etch that is selective of the metal base with respect to the conductive trace and the other conductive traces.

236. The method of claim 231, wherein etching the metal base removes all of the metal base that overlaps the conductive trace and the other conductive traces.

237. The method of claim 231, wherein etching the metal base removes all of the metal base that overlaps the chip.

238. The method of claim 231, wherein etching the metal base removes all of the metal base that overlaps the substrate.

239. The method of claim 231, wherein etching the metal base removes all of the metal base that overlaps the conductive trace, the other conductive traces, the chip and the substrate.

240. The method of claim 231, wherein etching the metal base removes the metal base.

241. The method of claim 1, including the following steps in the sequence set forth:

providing a metal base;

providing a plating mask on the metal base, wherein the plating mask includes an opening that exposes a portion of the metal base;

electroplating the conductive trace on the exposed portion of the metal base through the opening in the plating mask, wherein the conductive trace includes top and bottom surfaces, the top surface contacts the metal base, and the bottom surface is exposed;

removing the plating mask, thereby exposing peripheral sidewalls of the conductive trace between the top and bottom surfaces;

mechanically attaching the conductive trace to the chip and the substrate using an adhesive;

etching the metal base, thereby exposing the top surface and the adhesive;

removing selected portions of the adhesive, thereby exposing the conductive terminal and the pad; and

electrically connecting the conductive trace to the conductive terminal and the pad.

242. The method of claim 241, wherein mechanically attaching the conductive trace to the chip includes contacting the adhesive to the metal base.

243. The method of claim 241, wherein etching the metal base removes all of the metal base within a periphery of the conductive trace.

244. The method of claim 241, wherein etching the metal base removes all of the metal base within a periphery of the chip.

245. The method of claim 241, wherein etching the metal base removes all of the metal base within a periphery of the substrate.

246. The method of claim 241, wherein etching the metal base removes all of the metal base within a periphery of the conductive trace, the chip and the substrate.

247. The method of claim 241, wherein etching the metal base removes the metal base.

248. The method of claim 241, wherein the adhesive is coplanar with and adjacent to and contacts substantially none of the top surface and contacts the bottom surface and the peripheral sidewalls after mechanically attaching the conductive trace to the chip and the substrate and before etching the metal base.

249. The method of claim 241, wherein the plating mask is photoresist.

250. The method of claim 241, wherein the metal base is copper.

251. The method of claim 1, including the following steps in the sequence set forth:

providing a metal base;

providing a plating mask on the metal base, wherein the plating mask includes an opening that exposes a portion of the metal base;

electroplating the conductive trace on the exposed portion of the metal base through the opening in the plating mask, wherein the conductive trace includes top and bottom surfaces, the top surface contacts the metal base, and the bottom surface is exposed;

removing the plating mask, thereby exposing peripheral sidewalls of the conductive trace between the top and bottom surfaces;

mechanically attaching the conductive trace to the chip using a first adhesive;

etching the metal base using a first etch, thereby removing a selected portion of the metal base that overlaps a portion of the pad;

removing a selected portion of the first adhesive, thereby exposing the pad;

electrically connecting the conductive trace to the pad;

mechanically attaching the conductive trace and the chip to the substrate using a second adhesive;

etching the metal base using a second etch, thereby removing a selected portion of the metal base that overlaps a portion of the conductive terminal;

removing a selected portion of the second adhesive, thereby exposing the conductive terminal; and

electrically connecting the conductive trace to the conductive terminal.

252. The method of claim 251, wherein mechanically attaching the conductive trace to the chip includes contacting the first adhesive to the metal base.

253. The method of claim 251, wherein etching the metal base with the first etch removes all of the metal base within a periphery of the pad.

254. The method of claim 251, wherein etching the metal base with the first etch removes all of the metal base within a periphery of the chip.

255. The method of claim 251, wherein etching the metal base with the second etch removes all of the metal base within a periphery of the substrate.

256. The method of claim 251, wherein etching the metal base with the second etch removes all of the metal base within a periphery of the conductive trace, the chip and the substrate.

257. The method of claim 251, wherein etching the metal base with the second etch removes the metal base.

258. The method of claim 251, wherein the first adhesive is coplanar with and adjacent to and contacts substantially none of the top surface and contacts the bottom surface and the peripheral sidewalls after mechanically attaching the conductive trace to the chip and before etching the metal base with the first etch.

259. The method of claim 251, wherein the plating mask is photoresist.

260. The method of claim 251, wherein the metal base is copper.

261. The method of claim 1, including:

attaching the conductive trace to a metal base; then

disposing an adhesive between the conductive trace and the chip and between the conductive trace and the substrate, thereby mechanically attaching the conductive trace to the chip and the substrate; then

forming an opening that extends through the metal base and the adhesive and exposes the pad; then

forming a connection joint in the opening that contacts and electrically connects the conductive trace and the pad; and then

etching the metal base.

262. The method of claim 261, wherein attaching the conductive trace to the metal base includes electroplating the conductive trace on the metal base.

263. The method of claim 261, wherein disposing the adhesive includes contacting the adhesive to the metal base.

264. The method of claim 261, wherein forming the opening includes applying a wet chemical etch to the metal base.

265. The method of claim 261, wherein forming the opening includes applying a laser that ablates the adhesive.

266. The method of claim 261, wherein forming the connection joint includes depositing the connection joint on the metal base, the conductive trace and the pad.

267. The method of claim 261, wherein forming the connection joint includes electroplating the connection joint on the conductive trace and the pad.

268. The method of claim 261, wherein forming the connection joint includes electroplating the connection joint on the metal base, the conductive trace and the pad.

269. The method of claim 261, wherein forming the connection joint includes initially electroplating the connection joint on the metal base and the conductive trace, and then electroplating the connection joint on the pad.

270. The method of claim 261, wherein etching the metal base reduces contact area between the metal base and the connection joint.

271. The method of claim 1, including:

attaching the conductive trace to a metal base; then

disposing an adhesive between the conductive trace and the chip and between the conductive trace and the substrate, thereby mechanically attaching the conductive trace to the chip and the substrate; then

forming a via that extends through the metal base and the adhesive and exposes the conductive terminal; then

forming an interconnect in the via that contacts and electrically connects the conductive trace and the conductive terminal; and then

etching the metal base.

272. The method of claim 271, wherein attaching the conductive trace to the metal base includes electroplating the conductive trace on the metal base.

273. The method of claim 271, wherein disposing the adhesive includes contacting the adhesive to the metal base.

274. The method of claim 271, wherein forming the via includes applying a wet chemical etch to the metal base.

275. The method of claim 271, wherein forming the via includes applying a laser that ablates the adhesive.

276. The method of claim 271, wherein forming the interconnect includes depositing the interconnect on the metal base, the conductive trace and the conductive terminal.

277. The method of claim 271, wherein forming the interconnect includes electroplating the interconnect on the conductive trace and the conductive terminal.

278. The method of claim 271, wherein forming the interconnect includes electroplating the interconnect on the metal base, the conductive trace and the conductive terminal.

279. The method of claim 271, wherein forming the interconnect includes initially electroplating the interconnect on the metal base and the conductive trace, and then electroplating the interconnect on the conductive terminal.

280. The method of claim 271, wherein etching the metal base reduces contact area between the metal base and the interconnect.

281. The method of claim 1, including:

providing a structure that includes the conductive trace, an insulative base and a metal base, wherein the conductive trace and the metal base are disposed on opposite sides of the insulative base; then

disposing an adhesive between the conductive trace and the chip and between the conductive trace and the substrate, thereby mechanically attaching the conductive trace to the chip and the substrate; then

forming an opening that extends through the insulative base and the adhesive, thereby exposing the pad; and then

forming a connection joint in the opening that contacts and electrically connects the conductive trace and the pad.

282. The method of claim 281, wherein providing the conductive trace includes:

providing a metal layer that contacts the insulative base;

forming an etch mask on the metal layer; and

etching the metal layer using the etch mask to selectively protect the metal layer such that the conductive trace includes an unetched portion of the metal layer.

283. The method of claim 281, wherein disposing the adhesive includes contacting the adhesive to the insulative base.

284. The method of claim 281, wherein forming the opening includes applying a laser that ablates the insulative base and the adhesive.

285. The method of claim 281, wherein forming the connection joint includes electrolessly plating the connection joint on the conductive trace and the pad.

286. The method of claim 281, wherein forming the connection joint includes initially electrolessly plating the connection joint on the pad, and then electrolessly plating the connection joint on the conductive trace.

287. The method of claim 281, including etching the metal base, thereby exposing the insulative base after mechanically attaching the conductive trace to the chip and the substrate and before forming the opening.

288. The method of claim 287, wherein etching the metal base removes all of the metal base that overlaps the chip.

289. The method of claim 287, wherein etching the metal base removes all of the metal base that overlaps the substrate.

290. The method of claim 287, wherein etching the metal base removes the metal base.

291. The method of claim 1, including:

providing a structure that includes the conductive trace, an insulative base and a metal base, wherein the conductive trace and the metal base are disposed on opposite sides of the insulative base; then

disposing an adhesive between the conductive trace and the chip and between the conductive trace and the substrate, thereby mechanically attaching the conductive trace to the chip and the substrate; then

forming a via that extends through the insulative base and the adhesive, thereby exposing the conductive terminal; and then

forming an interconnect in the via that contacts and electrically connects the conductive trace and the conductive terminal.

292. The method of claim 291, wherein providing the conductive trace includes:

providing a metal layer that contacts the insulative base;

forming an etch mask on the metal layer; and

etching the metal layer using the etch mask to selectively protect the metal layer such that the conductive trace includes an unetched portion of the metal layer.

293. The method of claim 291, wherein disposing the adhesive includes contacting the adhesive to the insulative base.

294. The method of claim 291, wherein forming the via includes applying a laser that ablates the insulative base and the adhesive.

295. The method of claim 291, wherein forming the interconnect includes electrolessly plating the interconnect on the conductive trace and the conductive terminal.

296. The method of claim 291, wherein forming the interconnect includes initially electrolessly plating the interconnect on the conductive trace, and then electrolessly plating the interconnect on the conductive terminal.

297. The method of claim 291, including etching the metal base, thereby exposing the insulative base after mechanically attaching the conductive trace to the chip and the substrate and before forming the via.

298. The method of claim 297, wherein etching the metal base removes all of the metal base that overlaps the chip.

299. The method of claim 297, wherein etching the metal base removes all of the metal base that overlaps the substrate.

300. The method of claim 297, wherein etching the metal base removes the metal base.

301. A method of making a semiconductor chip assembly, comprising:

providing a semiconductor chip that includes first and second opposing major surfaces, wherein the first surface of the chip includes a conductive pad;

providing a conductive trace;

providing a substrate that includes first and second opposing major surfaces, wherein the first and second surfaces of the substrate include a conductive terminal and a dielectric base, the conductive terminal extends through the dielectric base and includes a first contact terminal at the first surface of the substrate and a second contact terminal at the second surface of the substrate, and a cavity extends from the first surface of the substrate into the substrate; then

mechanically attaching the conductive trace to the chip, the conductive trace to the substrate and the chip to the substrate using an adhesive, wherein the first surfaces

of the chip and the substrate face in a first direction, the second surfaces of the chip and the substrate face in a second direction, the second surface of the chip is disposed in the cavity, the conductive trace is disposed within and outside a periphery of the chip and outside the cavity, and the adhesive extends into the cavity; and then

electrically connecting the conductive trace to the conductive terminal and the pad, thereby electrically connecting the conductive terminal to the pad.

302. The method of claim 301, including contacting the adhesive to the conductive trace, then contacting the adhesive to the chip, and then hardening the adhesive.

303. The method of claim 301, including contacting the adhesive to the conductive trace, then contacting the adhesive to the substrate, and then hardening the adhesive.

304. The method of claim 301, including contacting the adhesive to the conductive trace, then contacting the adhesive to the chip, then contacting the adhesive to the substrate, and then hardening the adhesive.

305. The method of claim 301, including contacting a first adhesive to the conductive trace, then contacting the first adhesive to the chip, then contacting a second adhesive to the conductive trace and the first adhesive, then contacting the second adhesive to the substrate, and then hardening the first and second adhesives, wherein the adhesive includes the first and second adhesives.

306. The method of claim 305, including partially curing the first adhesive, thereby strengthening mechanical attachment between the conductive trace and the chip without strengthening mechanical attachment between the conductive trace and the substrate, then partially curing the second adhesive, thereby strengthening mechanical attachment between the conductive trace and the substrate, and then fully

curing the first and second adhesives, thereby strengthening mechanical attachment between the conductive trace, the chip and the substrate.

307. The method of claim 301, including contacting a first adhesive to the conductive trace, then contacting the first adhesive to the chip, then contacting a second adhesive to the substrate, then contacting the second adhesive to the conductive trace and the first adhesive, and then hardening the first and second adhesives, wherein the adhesive includes the first and second adhesives.

308. The method of claim 307, including partially curing the first adhesive, thereby strengthening mechanical attachment between the conductive trace and the chip without strengthening mechanical attachment between the conductive trace and the substrate, then partially curing the second adhesive, thereby strengthening mechanical attachment between the conductive trace and the substrate, and then fully curing the first and second adhesives, thereby strengthening mechanical attachment between the conductive trace, the chip and the substrate.

309. The method of claim 301, wherein the adhesive contacts and is sandwiched between the conductive trace and the pad, and the adhesive contacts and is sandwiched between the conductive trace and the first contact terminal after electrically connecting the conductive trace to the conductive terminal and the pad.

310. The method of claim 301, including forming an opening through the adhesive that exposes the pad, and then forming a connection joint in the opening that contacts and electrically connects the conductive trace and the pad.

311. The method of claim 301, including forming a via through the adhesive that exposes the first contact terminal, and then forming an interconnect in the via that contacts and electrically connects the conductive trace and the first contact terminal.

312. The method of claim 301, including forming an opening through the adhesive that exposes the pad and is disposed within the periphery of the chip, forming a via through the adhesive that exposes the first contact terminal and is disposed outside the periphery of the chip, forming a connection joint in the opening that contacts and electrically connects the conductive trace and the pad, and forming an interconnect in the via that contacts and electrically connects the conductive trace and the first contact terminal.

313. The method of claim 312, wherein forming the opening includes applying a laser that ablates the adhesive, and forming the via includes applying a laser that ablates the adhesive.

314. The method of claim 312, wherein forming the connection joint includes plating a metal on the conductive trace and the pad, and forming the interconnect includes plating a metal on the conductive trace and the first contact terminal.

315. The method of claim 312, including sequentially forming the opening and the via.

316. The method of claim 312, including simultaneously forming the connection joint and the interconnect.

317. The method of claim 312, including sequentially forming the opening and the via, and then simultaneously forming the connection joint and the interconnect during a plating operation.

318. The method of claim 312, wherein the connection joint and the interconnect are devoid of wire bonds and TAB leads.

319. The method of claim 312, wherein the conductive trace provides horizontal routing for the pad within and outside the periphery of the chip, the conductive terminal provides horizontal and vertical routing for the pad outside the periphery of the chip, the connection joint provides vertical routing for the pad within the periphery of the chip, and the interconnect provides vertical routing for the pad outside the periphery of the chip.

320. The method of claim 312, wherein the conductive trace provides fine-pitch fan-out routing for the pad, and the conductive terminal provides coarse-pitch fan-out routing for the pad.

321. A method of making a semiconductor chip assembly, comprising:

providing a semiconductor chip that includes first and second opposing major surfaces, wherein the first surface of the chip includes a conductive pad;

providing a conductive trace;

providing a substrate that includes first and second opposing major surfaces, wherein the first and second surfaces of the substrate include a conductive terminal and a dielectric base, the conductive terminal extends through the dielectric base and includes a first contact terminal at the first surface of the substrate and a second contact terminal at the second surface of the substrate, and a cavity extends from the first surface of the substrate into the substrate; then

mechanically attaching the conductive trace to the chip, the conductive trace to the substrate and the chip to the substrate using an adhesive, wherein the first surfaces of the chip and the substrate face in a first direction, the second surfaces of the chip and the substrate face in a second direction, the second surface of the chip is disposed in the cavity, and the conductive trace is disposed within and outside a periphery of the chip and outside the cavity; then

forming an opening that extends through the adhesive and exposes the pad;

forming a connection joint in the opening that contacts and electrically connects the conductive trace and the pad;

forming a via that extends through the adhesive and exposes the first contact terminal; and

forming an interconnect in the via that contacts and electrically connects the conductive trace and the first contact terminal.

322. The method of claim 321, wherein the first surface of the chip is disposed outside the cavity after mechanically attaching the chip to the substrate.

323. The method of claim 321, wherein the first surface of the chip is essentially coplanar with the first contact terminal after mechanically attaching the chip to the substrate.

324. The method of claim 321, wherein the second surface of the chip is spaced from the substrate by an open gap after mechanically attaching the chip to the substrate.

325. The method of claim 321, wherein the second surface of the chip is exposed after mechanically attaching the chip to the substrate.

326. The method of claim 321, wherein the conductive trace is essentially flat and parallel to the first surface of the chip and overlaps the pad and the first contact terminal after mechanically attaching the chip to the substrate.

327. The method of claim 321, wherein the conductive terminal is disposed outside the periphery of the chip after mechanically attaching the chip to the substrate.

328. The method of claim 321, wherein the adhesive is disposed between the conductive trace and the chip, the conductive trace and the substrate, and the chip and the substrate and extends into the cavity after mechanically attaching the chip to the substrate.

329. The method of claim 321, wherein the adhesive contacts and is sandwiched between the conductive trace and the pad after forming the connection joint, and the adhesive contacts and is sandwiched between the conductive trace and the first contact terminal after forming the interconnect.

330. The method of claim 321, wherein the cavity extends into but not through the substrate.

331. The method of claim 321, wherein the cavity extends through the substrate.

332. The method of claim 321, wherein the opening and the connection joint are disposed within the periphery of the chip, and the via and the interconnect are disposed outside the periphery of the chip.

333. The method of claim 321, wherein forming the opening includes applying a laser that ablates the adhesive, and forming the via includes applying a laser that ablates the adhesive.

334. The method of claim 321, wherein forming the connection joint includes plating a metal on the conductive trace and the pad, and forming the interconnect includes plating a metal on the conductive trace and the first contact terminal.

335. The method of claim 321, including sequentially forming the opening and the via.

336. The method of claim 321, including simultaneously forming the connection joint and the interconnect.

337. The method of claim 321, including sequentially forming the opening and the via, and then simultaneously forming the connection joint and the interconnect during a plating operation.

338. The method of claim 321, wherein the connection joint and the interconnect are devoid of wire bonds and TAB leads.

339. The method of claim 321, wherein the conductive trace provides horizontal routing for the pad within and outside the periphery of the chip, the conductive terminal provides horizontal and vertical routing for the pad outside the periphery of the chip, the connection joint provides vertical routing for the pad within the periphery of the chip, and the interconnect provides vertical routing for the pad outside the periphery of the chip.

340. The method of claim 321, wherein the conductive trace provides fine-pitch fan-out routing for the pad, and the conductive terminal provides coarse-pitch fan-out routing for the pad.

341. A method of making a semiconductor chip assembly, comprising:

providing a semiconductor chip that includes first and second opposing major surfaces, wherein the first surface of the chip includes a conductive pad;

providing a substrate that includes first and second opposing major surfaces, wherein the first and second surfaces of the substrate include a conductive terminal and a dielectric base, the conductive terminal extends through the dielectric base and includes a first contact terminal at the first surface of the substrate and a second contact terminal at the second surface of the substrate, and a cavity extends from the first surface of the substrate into the substrate;

depositing a conductive trace on a metal base; then

mechanically attaching the conductive trace to the chip, the conductive trace to the substrate and the chip to the substrate using an adhesive, wherein the first surfaces

of the chip and the substrate face in a first direction, the second surfaces of the chip and the substrate face in a second direction, the second surface of the chip is disposed in the cavity, and the conductive trace is disposed within and outside a periphery of the chip and outside the cavity; then

etching the metal base, thereby exposing the conductive trace and the adhesive;

forming an opening that extends through the adhesive and exposes the pad;

forming a connection joint in the opening that contacts and electrically connects the conductive trace and the pad;

forming a via that extends through the adhesive and exposes the first contact terminal; and

forming an interconnect in the via that contacts and electrically connects the conductive trace and the first contact terminal.

342. The method of claim 341, wherein the first surface of the chip is disposed outside the cavity after mechanically attaching the chip to the substrate.

343. The method of claim 341, wherein the first surface of the chip is essentially coplanar with the first contact terminal after mechanically attaching the chip to the substrate.

344. The method of claim 341, wherein the second surface of the chip is spaced from the substrate by an open gap after mechanically attaching the chip to the substrate.

345. The method of claim 341, wherein the second surface of the chip is exposed after mechanically attaching the chip to the substrate.

346. The method of claim 341, wherein the conductive trace is essentially flat and parallel to the first surface of the chip and overlaps the pad and the first contact terminal after mechanically attaching the chip to the substrate.

347. The method of claim 341, wherein the conductive terminal is disposed outside the periphery of the chip after mechanically attaching the chip to the substrate.

348. The method of claim 341, wherein the adhesive is disposed between the conductive trace and the chip, the conductive trace and the substrate, and the chip and the substrate and extends into the cavity after mechanically attaching the chip to the substrate.

349. The method of claim 341, wherein the adhesive contacts and is sandwiched between the conductive trace and the pad after forming the connection joint, and the adhesive contacts and is sandwiched between the conductive trace and the first contact terminal after forming the interconnect.

350. The method of claim 341, wherein the cavity extends into but not through the substrate.

351. The method of claim 341, wherein the cavity extends through the substrate.

352. The method of claim 341, wherein the opening and the connection joint are disposed within the periphery of the chip, and the via and the interconnect are disposed outside the periphery of the chip.

353. The method of claim 341, wherein forming the opening includes applying a laser that ablates the adhesive, and forming the via includes applying a laser that ablates the adhesive.

354. The method of claim 341, wherein forming the connection joint includes plating a metal on the conductive trace and the pad, and forming the interconnect includes plating a metal on the conductive trace and the first contact terminal.

355. The method of claim 341, including sequentially forming the opening and the via.

356. The method of claim 341, including simultaneously forming the connection joint and the interconnect.

357. The method of claim 341, including sequentially forming the opening and the via, and then simultaneously forming the connection joint and the interconnect during a plating operation.

358. The method of claim 341, wherein the connection joint and the interconnect are devoid of wire bonds and TAB leads.

359. The method of claim 341, wherein the conductive trace provides horizontal routing for the pad within and outside the periphery of the chip, the conductive terminal provides horizontal and vertical routing for the pad outside the periphery of the chip, the connection joint provides vertical routing for the pad within the periphery of the chip, and the interconnect provides vertical routing for the pad outside the periphery of the chip.

360. The method of claim 341, wherein the conductive trace provides fine-pitch fan-out routing for the pad, and the conductive terminal provides coarse-pitch fan-out routing for the pad.

361. A method of making a semiconductor chip assembly, comprising:

providing a semiconductor chip that includes first and second opposing major surfaces, wherein the first surface of the chip includes a conductive pad;

providing a laminated structure that includes a conductive trace, an insulative base and a metal base, wherein the conductive trace and the metal base are disposed on opposite sides of the insulative base;

providing a substrate that includes first and second opposing major surfaces, wherein the first and second surfaces of the substrate include a conductive terminal and a dielectric base, the conductive terminal extends through the dielectric base and includes a first contact terminal at the first surface of the substrate and a second contact terminal at the second surface of the substrate, and a cavity extends from the first surface of the substrate into the substrate; then

mechanically attaching the conductive trace to the chip, the conductive trace to the substrate and the chip to the substrate using an adhesive, wherein the first surfaces of the chip and the substrate face in a first direction, the second surfaces of the chip and the substrate face in a second direction, the second surface of the chip is disposed in the cavity, the conductive trace is disposed within and outside a periphery of the chip and outside the cavity, and the metal base covers and is electrically isolated from the conductive trace; then

etching the metal base, thereby exposing the insulative base;

forming an opening that extends through the insulative base and the adhesive and exposes the pad;

forming a connection joint in the opening that contacts and electrically connects the conductive trace and the pad;

forming a via that extends through the insulative base and the adhesive and exposes the first contact terminal; and

forming an interconnect in the via that contacts and electrically connects the conductive trace and the first contact terminal.

362. The method of claim 361, wherein the first surface of the chip is disposed outside the cavity after mechanically attaching the chip to the substrate.

363. The method of claim 361, wherein the first surface of the chip is essentially coplanar with the first contact terminal after mechanically attaching the chip to the substrate.

364. The method of claim 361, wherein the second surface of the chip is spaced from the substrate by an open gap after mechanically attaching the chip to the substrate.

365. The method of claim 361, wherein the second surface of the chip is exposed after mechanically attaching the chip to the substrate.

366. The method of claim 361, wherein the conductive trace is essentially flat and parallel to the first surface of the chip and overlaps the pad and the first contact terminal after mechanically attaching the chip to the substrate.

367. The method of claim 361, wherein the conductive terminal is disposed outside the periphery of the chip after mechanically attaching the chip to the substrate.

368. The method of claim 361, wherein the adhesive is disposed between the conductive trace and the chip, the conductive trace and the substrate, and the chip and the substrate and extends into the cavity after mechanically attaching the chip to the substrate.

369. The method of claim 361, wherein the adhesive contacts and is sandwiched between the conductive trace and the pad after forming the connection joint, and the adhesive contacts and is sandwiched between the conductive trace and the first contact terminal after forming the interconnect.

370. The method of claim 361, wherein the cavity extends into but not through the substrate.

371. The method of claim 361, wherein the cavity extends through the substrate.

372. The method of claim 361, wherein the opening and the connection joint are disposed within the periphery of the chip, and the via and the interconnect are disposed outside the periphery of the chip.

373. The method of claim 361, wherein forming the opening includes applying a laser that ablates the insulative base and the adhesive, and forming the via includes applying a laser that ablates the insulative base and the adhesive.

374. The method of claim 361, wherein forming the connection joint includes plating a metal on the conductive trace and the pad, and forming the interconnect includes plating a metal on the conductive trace and the first contact terminal.

375. The method of claim 361, including sequentially forming the opening and the via.

376. The method of claim 361, including simultaneously forming the connection joint and the interconnect.

377. The method of claim 361, including sequentially forming the opening and the via, and then simultaneously forming the connection joint and the interconnect during a plating operation.

378. The method of claim 361, wherein the connection joint and the interconnect are devoid of wire bonds and TAB leads.

379. The method of claim 361, wherein the conductive trace provides horizontal routing for the pad within and outside the periphery of the chip, the conductive terminal provides horizontal and vertical routing for the pad outside the periphery of the chip, the connection joint provides vertical routing for the pad within the periphery of the chip, and the interconnect provides vertical routing for the pad outside the periphery of the chip.

380. The method of claim 361, wherein the conductive trace provides fine-pitch fan-out routing for the pad, and the conductive terminal provides coarse-pitch fan-out routing for the pad.

381. A method of making a semiconductor chip assembly, comprising:

providing a semiconductor chip that includes first and second opposing major surfaces, wherein the first surface of the chip includes a conductive pad;

providing a conductive trace;

providing a substrate that includes first and second opposing major surfaces, wherein the first and second surfaces of the substrate include a conductive terminal and a dielectric base, the conductive terminal extends through the dielectric base and includes a first contact terminal at the first surface of the substrate and a second contact terminal at the second surface of the substrate, and a cavity extends from the first surface of the substrate into the substrate;

mechanically attaching the conductive trace to the chip, the conductive trace to the substrate and the chip to the substrate using an adhesive, wherein the first surfaces of the chip and the substrate face in a first direction, the second surfaces of the chip and the substrate face in a second direction, the second surface of the chip is disposed in the cavity, and the conductive trace is disposed within and outside a periphery of the chip and outside the cavity; and

electrically connecting the conductive trace to the conductive terminal and the pad, thereby electrically connecting the conductive terminal to the pad.

382. The method of claim 381, including contacting the adhesive to the conductive trace, then contacting the adhesive to the chip, and then hardening the adhesive.

383. The method of claim 381, including contacting the adhesive to the conductive trace, then contacting the adhesive to the substrate, and then hardening the adhesive.

384. The method of claim 381, including contacting the adhesive to the conductive trace, then contacting the adhesive to the chip, then contacting the adhesive to the substrate, and then hardening the adhesive.

385. The method of claim 381, including contacting a first adhesive to the conductive trace, then contacting the first adhesive to the chip, then contacting a second adhesive to the conductive trace and the first adhesive, and then contacting the second adhesive to the substrate, wherein the adhesive includes the first and second adhesives.

386. The method of claim 385, including fully curing the first adhesive, thereby strengthening mechanical attachment between the conductive trace and the chip without strengthening mechanical attachment between the conductive trace and the substrate, and then fully curing the second adhesive, thereby strengthening mechanical attachment between the conductive trace, the chip and the substrate.

387. The method of claim 381, including contacting a first adhesive to the conductive trace, then contacting the first adhesive to the chip, then contacting a second adhesive to the substrate, and then contacting the second adhesive to the conductive trace and the first adhesive, wherein the adhesive includes the first and second adhesives.

388. The method of claim 387, including fully curing the first adhesive, thereby strengthening mechanical attachment between the conductive trace and the chip without strengthening mechanical attachment between the conductive trace and the substrate, and then fully curing the second adhesive, thereby strengthening mechanical attachment between the conductive trace, the chip and the substrate.

389. The method of claim 381, wherein the adhesive contacts and is sandwiched between the conductive trace and the pad, and the adhesive contacts and is sandwiched between the conductive trace and the first contact terminal after electrically connecting the conductive trace to the conductive terminal and the pad.

390. The method of claim 381, wherein the assembly is devoid of wire bonds and TAB leads.

391. A method of making a semiconductor chip assembly, comprising:

providing a semiconductor chip that includes first and second opposing major surfaces, wherein the first surface of the chip includes a conductive pad;

providing a conductive trace;

providing a substrate that includes first and second opposing major surfaces, wherein the first and second surfaces of the substrate include a conductive terminal and a dielectric base, the conductive terminal extends through the dielectric base and includes a first contact terminal at the first surface of the substrate and a second contact terminal at the second surface of the substrate, and a cavity extends from the first surface of the substrate into the substrate and is spaced from the conductive terminal;

mechanically attaching the conductive trace to the chip, the conductive trace to the substrate and the chip to the substrate using an adhesive, wherein the first surfaces of the chip and the substrate face in a first direction, the second surfaces of the chip and the substrate face in a second direction, the second surface of the chip is disposed

in the cavity, the conductive trace is disposed within and outside a periphery of the chip and outside the cavity, and the adhesive is disposed between the conductive trace and the chip, the conductive trace and the substrate, and the chip and the substrate and extends into the cavity;

forming an opening that extends through the adhesive, is disposed within a periphery of the chip and exposes the pad;

forming a connection joint in the opening that contacts and electrically connects the conductive trace and the pad;

forming a via that extends through the adhesive, is disposed outside the periphery of the chip and exposes the first contact terminal; and

forming an interconnect in the via that contacts and electrically connects the conductive trace and the first contact terminal.

392. The method of claim 391, wherein the first surface of the chip is disposed outside the cavity after mechanically attaching the chip to the substrate.

393. The method of claim 391, wherein the first surface of the chip is essentially coplanar with the first contact terminal after mechanically attaching the chip to the substrate.

394. The method of claim 391, wherein the second surface of the chip is spaced from the substrate by an open gap after mechanically attaching the chip to the substrate.

395. The method of claim 391, wherein the second surface of the chip is exposed after mechanically attaching the chip to the substrate.

396. The method of claim 391, wherein the conductive trace is essentially flat and parallel to the first surface of the chip and overlaps the pad and the first contact terminal after mechanically attaching the chip to the substrate.

397. The method of claim 391, wherein the adhesive includes a first single-piece adhesive that contacts the conductive trace and the chip and is spaced from the substrate and a second single-piece adhesive that contacts the conductive trace, the substrate and the first single-piece adhesive after mechanically attaching the chip to the substrate.

398. The method of claim 391, wherein the cavity extends into but not through the substrate.

399. The method of claim 391, wherein the cavity extends through the substrate.

400. The method of claim 391, wherein the assembly is devoid of wire bonds and TAB leads.

401. A method of making a semiconductor chip assembly, comprising:

providing a semiconductor chip that includes first and second opposing major surfaces, wherein the first surface of the chip includes a conductive pad;

providing a substrate that includes first and second opposing major surfaces, wherein the first and second surfaces of the substrate include a conductive terminal and a dielectric base, the conductive terminal extends through the dielectric base and includes a first contact terminal at the first surface of the substrate and a second contact terminal at the second surface of the substrate, and a cavity extends from the first surface of the substrate into the substrate and is spaced from the conductive terminal;

depositing a conductive trace on a metal base; then

mechanically attaching the conductive trace to the chip, the conductive trace to the substrate and the chip to the substrate using an adhesive, wherein the first surfaces of the chip and the substrate face in a first direction, the second surfaces of the chip

and the substrate face in a second direction, the second surface of the chip is disposed in the cavity, the conductive trace is disposed within and outside a periphery of the chip and outside the cavity, and the adhesive is disposed between the conductive trace and the chip, the conductive trace and the substrate, and the chip and the substrate and extends into the cavity;

etching the metal base, thereby exposing the conductive trace and the adhesive;

forming an opening that extends through the adhesive and exposes the pad;

forming a connection joint in the opening that contacts and electrically connects the conductive trace and the pad;

forming a via that extends through the adhesive and exposes the first contact terminal; and

forming an interconnect in the via that contacts and electrically connects the conductive trace and the first contact terminal.

402. The method of claim 401, wherein the first surface of the chip is disposed outside the cavity after mechanically attaching the chip to the substrate.

403. The method of claim 401, wherein the first surface of the chip is essentially coplanar with the first contact terminal after mechanically attaching the chip to the substrate.

404. The method of claim 401, wherein the second surface of the chip is spaced from the substrate by an open gap after mechanically attaching the chip to the substrate.

405. The method of claim 401, wherein the second surface of the chip is exposed after mechanically attaching the chip to the substrate.

406. The method of claim 401, wherein the conductive trace is essentially flat and parallel to the first surface of the chip and overlaps the pad and the first contact terminal after mechanically attaching the chip to the substrate.

407. The method of claim 401, wherein the adhesive includes a first single-piece adhesive that contacts the conductive trace and the chip and is spaced from the substrate and a second single-piece adhesive that contacts the conductive trace, the substrate and the first single-piece adhesive after mechanically attaching the chip to the substrate.

408. The method of claim 401, wherein the cavity extends into but not through the substrate.

409. The method of claim 401, wherein the cavity extends through the substrate.

410. The method of claim 401, wherein the assembly is devoid of wire bonds and TAB leads.

411. A method of making a semiconductor chip assembly, comprising:

providing a semiconductor chip that includes first and second opposing major surfaces, wherein the first surface of the chip includes a conductive pad;

providing a laminated structure that includes a conductive trace, an insulative base and a metal base, wherein the conductive trace and the metal base are disposed on opposite sides of the insulative base;

providing a substrate that includes first and second opposing major surfaces, wherein the first and second surfaces of the substrate include a conductive terminal and a dielectric base, the conductive terminal extends through the dielectric base and includes a first contact terminal at the first surface of the substrate and a second

contact terminal at the second surface of the substrate, and a cavity extends from the first surface of the substrate into the substrate; then

mechanically attaching the conductive trace to the chip, the conductive trace to the substrate and the chip to the substrate using an adhesive, wherein the first surfaces of the chip and the substrate face in a first direction, the second surfaces of the chip and the substrate face in a second direction, the second surface of the chip is disposed in the cavity, the conductive trace is disposed within and outside a periphery of the chip and outside the cavity, the metal base covers and is electrically isolated from the conductive trace, and the adhesive is disposed between the conductive trace and the chip, the conductive trace and the substrate, and the chip and the substrate and extends into the cavity;

etching the metal base, thereby exposing the insulative base;

forming an opening that extends through the insulative base and the adhesive and exposes the pad;

forming a connection joint in the opening that contacts and electrically connects the conductive trace and the pad;

forming a via that extends through the insulative base and the adhesive and exposes the first contact terminal; and

forming an interconnect in the via that contacts and electrically connects the conductive trace and the first contact terminal.

412. The method of claim 411, wherein the first surface of the chip is disposed outside the cavity after mechanically attaching the chip to the substrate.

413. The method of claim 411, wherein the first surface of the chip is essentially coplanar with the first contact terminal after mechanically attaching the chip to the substrate.

414. The method of claim 411, wherein the second surface of the chip is spaced from the substrate by an open gap after mechanically attaching the chip to the substrate.

415. The method of claim 411, wherein the second surface of the chip is exposed after mechanically attaching the chip to the substrate.

416. The method of claim 411, wherein the conductive trace is essentially flat and parallel to the first surface of the chip and overlaps the pad and the first contact terminal after mechanically attaching the chip to the substrate.

417. The method of claim 411, wherein the adhesive includes a first single-piece adhesive that contacts the conductive trace, the insulative base and the chip and is spaced from the substrate and a second single-piece adhesive that contacts the conductive trace, the insulative base, the substrate and the first single-piece adhesive after mechanically attaching the chip to the substrate.

418. The method of claim 411, wherein the cavity extends into but not through the substrate.

419. The method of claim 411, wherein the cavity extends through the substrate.

420. The method of claim 411, wherein the assembly is devoid of wire bonds and TAB leads.

421. A method of making a semiconductor chip assembly, comprising:

providing a semiconductor chip that includes first and second opposing major surfaces, wherein the first surface of the chip includes a conductive pad;

providing a conductive trace;

providing a substrate that includes first and second opposing major surfaces, wherein the first and second surfaces of the substrate include a conductive terminal and a dielectric base, the conductive terminal extends through the dielectric base and includes a first contact terminal at the first surface of the substrate and a second contact terminal at the second surface of the substrate, and a cavity extends from the first surface of the substrate into the substrate;

disposing an adhesive between the conductive trace and the chip, the conductive trace and the substrate, and the chip and the substrate;

hardening the adhesive, thereby transforming a loose mechanical bond between the conductive trace and the chip, the conductive trace and the substrate, and the chip and the substrate into a solid mechanical bond between the conductive trace and the chip, the conductive trace and the substrate, and the chip and the substrate, wherein the first surfaces of the chip and the substrate face in a first direction, the second surfaces of the chip and the substrate face in a second direction, the chip extends into the cavity, and the conductive trace is disposed within and outside a periphery of the chip and outside the cavity; and

electrically connecting the conductive trace to the conductive terminal and the pad, thereby electrically connecting the conductive terminal to the pad.

422. The method of claim 421, including electrically connecting the conductive trace to the pad, then mechanically attaching the chip to the substrate, and then electrically connecting the conductive trace to the conductive terminal.

423. The method of claim 421, including:

forming an opening that extends through the adhesive and exposes the pad;

forming a connection joint in the opening that contacts and electrically connects the conductive trace and the pad;

forming a via that extends through the adhesive and exposes the first contact terminal; and

forming an interconnect in the via that contacts and electrically connects the conductive trace and the first contact terminal.

424. The method of claim 423, wherein forming the connection joint includes plating a metal on the conductive trace and the pad, and forming the interconnect includes depositing solder or conductive adhesive on the conductive trace and the first contact terminal.

425. The method of claim 423, wherein the conductive trace provides horizontal routing for the pad within and outside the periphery of the chip, the conductive terminal provides horizontal and vertical routing for the pad outside the periphery of the chip, the connection joint provides vertical routing for the pad within the periphery of the chip, and the interconnect provides vertical routing for the pad outside the periphery of the chip.

426. A method of making a semiconductor chip assembly, comprising:

providing a semiconductor chip that includes first and second opposing major surfaces, wherein the first surface of the chip includes a conductive pad;

providing a conductive trace;

providing a substrate that includes first and second opposing major surfaces, wherein the first and second surfaces of the substrate include a conductive terminal and a dielectric base, the conductive terminal extends through the dielectric base and includes a first contact terminal at the first surface of the substrate and a second contact terminal at the second surface of the substrate, and a cavity extends from the first surface of the substrate into the substrate; then

disposing an adhesive between the conductive trace and the chip, the conductive trace and the substrate, and the chip and the substrate; then

hardening the adhesive, thereby transforming a loose mechanical bond between the conductive trace and the chip, the conductive trace and the substrate, and the chip and the substrate into a solid mechanical bond between the conductive trace and the

chip, the conductive trace and the substrate, and the chip and the substrate, wherein the first surfaces of the chip and the substrate face in a first direction, the second surfaces of the chip and the substrate face in a second direction, the chip extends into the cavity, and the conductive trace is disposed within and outside a periphery of the chip and outside the cavity; and then

electrically connecting the conductive trace to the conductive terminal and the pad, thereby electrically connecting the conductive terminal to the pad.

427. The method of claim 426, including:

forming an opening that extends through the adhesive and exposes the pad;

forming a connection joint in the opening that contacts and electrically connects the conductive trace and the pad;

forming a via that extends through the adhesive and exposes the first contact terminal; and

forming an interconnect in the via that contacts and electrically connects the conductive trace and the first contact terminal.

428. The method of claim 427, wherein forming the connection joint includes plating a metal on the conductive trace and the pad during a plating operation, and forming the interconnect includes plating a metal on the conductive trace and the first contact terminal during the plating operation.

429. The method of claim 427, wherein forming the connection joint includes plating a metal on the conductive trace and the pad, and forming the interconnect includes depositing solder or conductive adhesive on the conductive trace and the first contact terminal.

430. The method of claim 427, wherein the conductive trace provides horizontal routing for the pad within and outside the periphery of the chip, the conductive terminal provides horizontal and vertical routing for the pad outside the

periphery of the chip, the connection joint provides vertical routing for the pad within the periphery of the chip, and the interconnect provides vertical routing for the pad outside the periphery of the chip.

431. A method of making a semiconductor chip assembly, comprising:

providing a semiconductor chip that includes first and second opposing major surfaces, wherein the first surface of the chip includes a conductive pad;

providing a conductive trace;

providing a substrate that includes first and second opposing major surfaces, wherein the first and second surfaces of the substrate include a conductive terminal and a dielectric base, the conductive terminal extends through the dielectric base and includes a first contact terminal at the first surface of the substrate and a second contact terminal at the second surface of the substrate, and a cavity extends from the first surface of the substrate into the substrate;

disposing an adhesive between the conductive trace and the chip, the conductive trace and the substrate, and the chip and the substrate;

hardening the adhesive, wherein the first surfaces of the chip and the substrate face in a first direction, the second surfaces of the chip and the substrate face in a second direction, the chip extends into the cavity, the chip and the adhesive seal the cavity at the first surface of the substrate, and the conductive trace is disposed within and outside a periphery of the chip and outside the cavity; and

electrically connecting the conductive trace to the conductive terminal and the pad, thereby electrically connecting the conductive terminal to the pad.

432. The method of claim 431, including electrically connecting the conductive trace to the pad, then mechanically attaching the chip to the substrate, and then electrically connecting the conductive trace to the conductive terminal.

433. The method of claim 431, including:

forming an opening that extends through the adhesive and exposes the pad;

forming a connection joint in the opening that contacts and electrically connects the conductive trace and the pad;

forming a via that extends through the adhesive and exposes the first contact terminal; and

forming an interconnect in the via that contacts and electrically connects the conductive trace and the first contact terminal.

434. The method of claim 433, wherein forming the connection joint includes plating a metal on the conductive trace and the pad, and forming the interconnect includes depositing solder or conductive adhesive on the conductive trace and the first contact terminal.

435. The method of claim 433, wherein the conductive trace provides horizontal routing for the pad within and outside the periphery of the chip, the conductive terminal provides horizontal and vertical routing for the pad outside the periphery of the chip, the connection joint provides vertical routing for the pad within the periphery of the chip, and the interconnect provides vertical routing for the pad outside the periphery of the chip.

436. A method of making a semiconductor chip assembly, comprising:

providing a semiconductor chip that includes first and second opposing major surfaces, wherein the first surface of the chip includes a conductive pad;

providing a conductive trace;

providing a substrate that includes first and second opposing major surfaces, wherein the first and second surfaces of the substrate include a conductive terminal and a dielectric base, the conductive terminal extends through the dielectric base and includes a first contact terminal at the first surface of the substrate and a second contact terminal at the second surface of the substrate, and a cavity extends from the first surface of the substrate into the substrate; then

disposing an adhesive between the conductive trace and the chip, the conductive trace and the substrate, and the chip and the substrate; then

hardening the adhesive, wherein the first surfaces of the chip and the substrate face in a first direction, the second surfaces of the chip and the substrate face in a second direction, the chip extends into the cavity, the chip and the adhesive seal the cavity at the first surface of the substrate, and the conductive trace is disposed within and outside a periphery of the chip and outside the cavity; and then

electrically connecting the conductive trace to the conductive terminal and the pad, thereby electrically connecting the conductive terminal to the pad.

437. The method of claim 436, including:

forming an opening that extends through the adhesive and exposes the pad;

forming a connection joint in the opening that contacts and electrically connects the conductive trace and the pad;

forming a via that extends through the adhesive and exposes the first contact terminal; and

forming an interconnect in the via that contacts and electrically connects the conductive trace and the first contact terminal.

438. The method of claim 437, wherein forming the connection joint includes plating a metal on the conductive trace and the pad during a plating operation, and forming the interconnect includes plating a metal on the conductive trace and the first contact terminal during the plating operation.

439. The method of claim 437, wherein forming the connection joint includes plating a metal on the conductive trace and the pad, and forming the interconnect includes depositing solder or conductive adhesive on the conductive trace and the first contact terminal.

440. The method of claim 437, wherein the conductive trace provides horizontal routing for the pad within and outside the periphery of the chip, the conductive terminal provides horizontal and vertical routing for the pad outside the periphery of the chip, the connection joint provides vertical routing for the pad within the periphery of the chip, and the interconnect provides vertical routing for the pad outside the periphery of the chip.

441. A method of making a semiconductor chip assembly, comprising:

providing a semiconductor chip that includes first and second opposing major surfaces, wherein the first surface of the chip includes a conductive pad;

providing a conductive trace;

providing a substrate that includes first and second opposing major surfaces, wherein the first and second surfaces of the substrate include a conductive terminal and a dielectric base, the conductive terminal extends through the dielectric base and includes a first contact terminal at the first surface of the substrate and a second contact terminal at the second surface of the substrate, and a cavity extends from the first surface of the substrate into the substrate;

mechanically attaching the chip to the substrate without applying pressure to the second surface of the chip, wherein the first surfaces of the chip and the substrate face in a first direction, the second surfaces of the chip and the substrate face in a second direction, the second surface of the chip is disposed in the cavity, the cavity is sealed at the first surface of the substrate, and the conductive trace is mechanically attached to the chip and the substrate and disposed within and outside a periphery of the chip and outside the cavity; and

electrically connecting the conductive trace to the conductive terminal and the pad, thereby electrically connecting the conductive terminal to the pad.

442. The method of claim 441, including electrically connecting the conductive trace to the pad, then mechanically attaching the chip to the substrate, and then electrically connecting the conductive trace to the conductive terminal.

443. The method of claim 441, including:

forming an opening that extends through an adhesive and exposes the pad;

forming a connection joint in the opening that contacts and electrically connects the conductive trace and the pad;

forming a via that extends through the adhesive and exposes the first contact terminal; and

forming an interconnect in the via that contacts and electrically connects the conductive trace and the first contact terminal.

444. The method of claim 443, wherein forming the connection joint includes plating a metal on the conductive trace and the pad, and forming the interconnect includes depositing solder or conductive adhesive on the conductive trace and the first contact terminal.

445. The method of claim 443, wherein the conductive trace provides horizontal routing for the pad within and outside the periphery of the chip, the conductive terminal provides horizontal and vertical routing for the pad outside the periphery of the chip, the connection joint provides vertical routing for the pad within the periphery of the chip, and the interconnect provides vertical routing for the pad outside the periphery of the chip.

446. A method of making a semiconductor chip assembly, comprising:

providing a semiconductor chip that includes first and second opposing major surfaces, wherein the first surface of the chip includes a conductive pad;

providing a conductive trace;

providing a substrate that includes first and second opposing major surfaces, wherein the first and second surfaces of the substrate include a conductive terminal and a dielectric base, the conductive terminal extends through the dielectric base and includes a first contact terminal at the first surface of the substrate and a second

contact terminal at the second surface of the substrate, and a cavity extends from the first surface of the substrate into the substrate; then

mechanically attaching the chip to the substrate without applying pressure to the second surface of the chip, wherein the first surfaces of the chip and the substrate face in a first direction, the second surfaces of the chip and the substrate face in a second direction, the second surface of the chip is disposed in the cavity, the cavity is sealed at the first surface of the substrate, and the conductive trace is mechanically attached to the chip and the substrate and disposed within and outside a periphery of the chip and outside the cavity; and then

electrically connecting the conductive trace to the conductive terminal and the pad, thereby electrically connecting the conductive terminal to the pad.

447. The method of claim 446, including:

forming an opening that extends through an adhesive and exposes the pad;

forming a connection joint in the opening that contacts and electrically connects the conductive trace and the pad;

forming a via that extends through the adhesive and exposes the first contact terminal; and

forming an interconnect in the via that contacts and electrically connects the conductive trace and the first contact terminal.

448. The method of claim 447, wherein forming the connection joint includes plating a metal on the conductive trace and the pad during a plating operation, and forming the interconnect includes plating a metal on the conductive trace and the first contact terminal during the plating operation.

449. The method of claim 447, wherein forming the connection joint includes plating a metal on the conductive trace and the pad, and forming the interconnect includes depositing solder or conductive adhesive on the conductive trace and the first contact terminal.

450. The method of claim 447, wherein the conductive trace provides horizontal routing for the pad within and outside the periphery of the chip, the conductive terminal provides horizontal and vertical routing for the pad outside the periphery of the chip, the connection joint provides vertical routing for the pad within the periphery of the chip, and the interconnect provides vertical routing for the pad outside the periphery of the chip.

451. A method of making a semiconductor chip assembly, comprising:

providing a semiconductor chip that includes first and second opposing major surfaces, wherein the first surface of the chip includes a conductive pad;

providing a conductive trace;

providing a substrate that includes first and second opposing major surfaces, wherein the first and second surfaces of the substrate include a conductive terminal and a dielectric base, the conductive terminal extends through the dielectric base and includes a first contact terminal at the first surface of the substrate and a second contact terminal at the second surface of the substrate, and a cavity extends from the first surface of the substrate into the substrate;

mechanically attaching the chip to the substrate, wherein the first surfaces of the chip and the substrate face in a first direction, the second surfaces of the chip and the substrate face in a second direction, the second surface of the chip is disposed in the cavity, the conductive trace is mechanically attached to the chip and the substrate and disposed within and outside a periphery of the chip and outside the cavity, and an open gap in the cavity intersects an imaginary line between the second surfaces of the chip and the substrate and does not intersect an imaginary line between the first surfaces of the chip and the substrate; and

electrically connecting the conductive trace to the conductive terminal and the pad, thereby electrically connecting the conductive terminal to the pad.

452. The method of claim 451, including electrically connecting the conductive trace to the pad, then mechanically attaching the chip to the substrate, and then electrically connecting the conductive trace to the conductive terminal.

453. The method of claim 451, including:

forming an opening that extends through an adhesive and exposes the pad;

forming a connection joint in the opening that contacts and electrically connects the conductive trace and the pad;

forming a via that extends through the adhesive and exposes the first contact terminal; and

forming an interconnect in the via that contacts and electrically connects the conductive trace and the first contact terminal.

454. The method of claim 453, wherein forming the connection joint includes plating a metal on the conductive trace and the pad, and forming the interconnect includes depositing solder or conductive adhesive on the conductive trace and the first contact terminal.

455. The method of claim 453, wherein the conductive trace provides horizontal routing for the pad within and outside the periphery of the chip, the conductive terminal provides horizontal and vertical routing for the pad outside the periphery of the chip, the connection joint provides vertical routing for the pad within the periphery of the chip, and the interconnect provides vertical routing for the pad outside the periphery of the chip.

456. A method of making a semiconductor chip assembly, comprising:

providing a semiconductor chip that includes first and second opposing major surfaces, wherein the first surface of the chip includes a conductive pad;

providing a conductive trace;

providing a substrate that includes first and second opposing major surfaces, wherein the first and second surfaces of the substrate include a conductive terminal and a dielectric base, the conductive terminal extends through the dielectric base and includes a first contact terminal at the first surface of the substrate and a second contact terminal at the second surface of the substrate, and a cavity extends from the first surface of the substrate into the substrate; then

mechanically attaching the chip to the substrate, wherein the first surfaces of the chip and the substrate face in a first direction, the second surfaces of the chip and the substrate face in a second direction, the second surface of the chip is disposed in the cavity, the conductive trace is mechanically attached to the chip and the substrate and disposed within and outside a periphery of the chip and outside the cavity, and an open gap in the cavity intersects an imaginary line between the second surfaces of the chip and the substrate and does not intersect an imaginary line between the first surfaces of the chip and the substrate; and then

electrically connecting the conductive trace to the conductive terminal and the pad, thereby electrically connecting the conductive terminal to the pad.

457. The method of claim 456, including:

forming an opening that extends through an adhesive and exposes the pad;

forming a connection joint in the opening that contacts and electrically connects the conductive trace and the pad;

forming a via that extends through the adhesive and exposes the first contact terminal; and

forming an interconnect in the via that contacts and electrically connects the conductive trace and the first contact terminal.

458. The method of claim 457, wherein forming the connection joint includes plating a metal on the conductive trace and the pad during a plating operation, and forming the interconnect includes plating a metal on the conductive trace and the first contact terminal during the plating operation.

459. The method of claim 457, wherein forming the connection joint includes plating a metal on the conductive trace and the pad, and forming the interconnect includes depositing solder or conductive adhesive on the conductive trace and the first contact terminal.

460. The method of claim 457, wherein the conductive trace provides horizontal routing for the pad within and outside the periphery of the chip, the conductive terminal provides horizontal and vertical routing for the pad outside the periphery of the chip, the connection joint provides vertical routing for the pad within the periphery of the chip, and the interconnect provides vertical routing for the pad outside the periphery of the chip.

461. A method of making a semiconductor chip assembly, comprising:

providing a semiconductor chip that includes first and second opposing major surfaces, wherein the first surface of the chip includes a conductive pad;

providing a conductive trace;

providing a substrate that includes first and second opposing major surfaces, wherein the first and second surfaces of the substrate include a conductive terminal and a dielectric base, the conductive terminal extends through the dielectric base and includes a first contact terminal at the first surface of the substrate and a second contact terminal at the second surface of the substrate, and a cavity extends from the first surface of the substrate into the substrate;

mechanically attaching the conductive trace to the chip, the conductive trace to the substrate and the chip to the substrate, wherein the first surfaces of the chip and the substrate face in a first direction, the second surfaces of the chip and the substrate face in a second direction, the chip extends into the cavity, and the conductive trace is disposed within and outside a periphery of the chip and outside the cavity; and

electrically connecting the conductive trace to the conductive terminal and the pad, thereby electrically connecting the conductive terminal to the pad, wherein the

conductive trace is electrically connected to the pad during a plating operation, and the conductive trace is not electrically connected to the conductive terminal during the plating operation.

462. The method of claim 461, including electrically connecting the conductive trace to the pad, then mechanically attaching the chip to the substrate, and then electrically connecting the conductive trace to the conductive terminal.

463. The method of claim 461, including:

forming an opening that extends through an adhesive and exposes the pad;

forming a connection joint in the opening that contacts and electrically connects the conductive trace and the pad;

forming a via that extends through the adhesive and exposes the first contact terminal; and

forming an interconnect in the via that contacts and electrically connects the conductive trace and the first contact terminal.

464. The method of claim 463, wherein forming the connection joint includes plating a metal on the conductive trace and the pad during the plating operation, and forming the interconnect includes depositing solder or conductive adhesive on the conductive trace and the first contact terminal.

465. The method of claim 463, wherein the conductive trace provides horizontal routing for the pad within and outside the periphery of the chip, the conductive terminal provides horizontal and vertical routing for the pad outside the periphery of the chip, the connection joint provides vertical routing for the pad within the periphery of the chip, and the interconnect provides vertical routing for the pad outside the periphery of the chip.

466. A method of making a semiconductor chip assembly, comprising:

providing a semiconductor chip that includes first and second opposing major surfaces, wherein the first surface of the chip includes a conductive pad;

providing a conductive trace;

providing a substrate that includes first and second opposing major surfaces, wherein the first and second surfaces of the substrate include a conductive terminal and a dielectric base, the conductive terminal extends through the dielectric base and includes a first contact terminal at the first surface of the substrate and a second contact terminal at the second surface of the substrate, and a cavity extends from the first surface of the substrate into the substrate; then

mechanically attaching the conductive trace to the chip, the conductive trace to the substrate and the chip to the substrate, wherein the first surfaces of the chip and the substrate face in a first direction, the second surfaces of the chip and the substrate face in a second direction, the chip extends into the cavity, and the conductive trace is disposed within and outside a periphery of the chip and outside the cavity; and then

electrically connecting the conductive trace to the conductive terminal and the pad during a plating operation, thereby electrically connecting the conductive terminal to the pad.

467. The method of claim 466, including:

forming an opening that extends through an adhesive and exposes the pad;

forming a connection joint in the opening that contacts and electrically connects the conductive trace and the pad;

forming a via that extends through the adhesive and exposes the first contact terminal; and

forming an interconnect in the via that contacts and electrically connects the conductive trace and the first contact terminal.

468. The method of claim 467, wherein the adhesive is disposed between the conductive trace and the chip, the conductive trace and the substrate, and the chip and the substrate after mechanically attaching the chip to the substrate.

469. The method of claim 467, wherein forming the connection joint includes plating a metal on the conductive trace and the pad during the plating operation, and forming the interconnect includes plating a metal on the conductive trace and the first contact terminal during the plating operation.

470. The method of claim 467, wherein the conductive trace provides horizontal routing for the pad within and outside the periphery of the chip, the conductive terminal provides horizontal and vertical routing for the pad outside the periphery of the chip, the connection joint provides vertical routing for the pad within the periphery of the chip, and the interconnect provides vertical routing for the pad outside the periphery of the chip.

471. A method of making a semiconductor chip assembly, comprising:

providing a semiconductor chip that includes first and second opposing major surfaces, wherein the first surface of the chip includes a conductive pad;

providing a structure that includes a conductive trace and a metal base;

providing a substrate that includes first and second opposing major surfaces, wherein the first and second surfaces of the substrate include a conductive terminal and a dielectric base, the conductive terminal extends through the dielectric base and includes a first contact terminal at the first surface of the substrate and a second contact terminal at the second surface of the substrate, and a cavity extends from the first surface of the substrate into the substrate;

mechanically attaching the conductive trace and the metal base to the chip, the conductive trace and the metal base to the substrate and the chip to the substrate, wherein the first surfaces of the chip and the substrate face in a first direction towards the metal base, the second surfaces of the chip and the substrate face in a second direction away from the metal base, the chip extends into the cavity, the conductive trace is disposed within and outside a periphery of the chip and outside the cavity, and the metal base is covers the entire periphery of the substrate;

removing most or all of the metal base within the periphery of the substrate; and

electrically connecting the conductive trace to the conductive terminal and the pad, thereby electrically connecting the conductive terminal to the pad.

472. The method of claim 471, including electrically connecting the conductive trace to the pad, then mechanically attaching the chip to the substrate, and then electrically connecting the conductive trace to the conductive terminal.

473. The method of claim 471, including:

forming an opening that extends through an adhesive and exposes the pad;

forming a connection joint in the opening that contacts and electrically connects the conductive trace and the pad;

forming a via that extends through the adhesive and exposes the first contact terminal; and

forming an interconnect in the via that contacts and electrically connects the conductive trace and the first contact terminal.

474. The method of claim 473, wherein forming the connection joint includes plating a metal on the conductive trace and the pad, and forming the interconnect includes depositing solder or conductive adhesive on the conductive trace and the first contact terminal.

475. The method of claim 473, wherein the conductive trace provides horizontal routing for the pad within and outside the periphery of the chip, the conductive terminal provides horizontal and vertical routing for the pad outside the periphery of the chip, the connection joint provides vertical routing for the pad within the periphery of the chip, and the interconnect provides vertical routing for the pad outside the periphery of the chip.

476. A method of making a semiconductor chip assembly, comprising:

providing a semiconductor chip that includes first and second opposing major surfaces, wherein the first surface of the chip includes a conductive pad;

providing a structure that includes a conductive trace and a metal base;

providing a substrate that includes first and second opposing major surfaces, wherein the first and second surfaces of the substrate include a conductive terminal and a dielectric base, the conductive terminal extends through the dielectric base and includes a first contact terminal at the first surface of the substrate and a second contact terminal at the second surface of the substrate, and a cavity extends from the first surface of the substrate into the substrate; then

mechanically attaching the conductive trace and the metal base to the chip, the conductive trace and the metal base to the substrate and the chip to the substrate, wherein the first surfaces of the chip and the substrate face in a first direction towards the metal base, the second surfaces of the chip and the substrate face in a second direction away from the metal base, the chip extends into the cavity, the conductive trace is disposed within and outside a periphery of the chip and outside the cavity, and the metal base is disposed within and outside the periphery of the chip and covers the entire periphery of the chip and the substrate; then

removing most or all of the metal base within the periphery of the chip and the substrate; and

electrically connecting the conductive trace to the conductive terminal and the pad, thereby electrically connecting the conductive terminal to the pad.

477. The method of claim 476, including:

forming an opening that extends through an adhesive and exposes the pad;

forming a connection joint in the opening that contacts and electrically connects the conductive trace and the pad;

forming a via that extends through the adhesive and exposes the first contact terminal; and

forming an interconnect in the via that contacts and electrically connects the conductive trace and the first contact terminal.

478. The method of claim 477, wherein forming the connection joint includes plating a metal on the conductive trace and the pad during a plating operation, and forming the interconnect includes plating a metal on the conductive trace and the first contact terminal during the plating operation.

479. The method of claim 477, wherein forming the connection joint includes plating a metal on the conductive trace and the pad, and forming the interconnect includes depositing solder or conductive adhesive on the conductive trace and the first contact terminal.

480. The method of claim 477, wherein the conductive trace provides horizontal routing for the pad within and outside the periphery of the chip, the conductive terminal provides horizontal and vertical routing for the pad outside the periphery of the chip, the connection joint provides vertical routing for the pad within the periphery of the chip, and the interconnect provides vertical routing for the pad outside the periphery of the chip.

481. A method of making a semiconductor chip assembly, comprising:

providing a semiconductor chip that includes first and second opposing major surfaces, wherein the first surface of the chip includes a conductive pad;

providing a conductive trace;

providing a substrate that includes first and second opposing major surfaces, wherein the first and second surfaces of the substrate include a conductive terminal and a dielectric base, the conductive terminal extends through the dielectric base and includes a first contact terminal at the first surface of the substrate and a second contact terminal at the second surface of the substrate, and a cavity extends from the first surface of the substrate into the substrate;

aligning the chip with the conductive trace;

forming a connection joint that contacts and electrically connects the conductive trace and the pad;

aligning the substrate with the conductive trace and the chip, wherein the first surfaces of the chip and the substrate face in a first direction, the second surfaces of the chip and the substrate face in a second direction, the chip extends into the cavity, the conductive trace is disposed within and outside a periphery of the chip and outside the cavity, and an interconnect that includes solder is disposed between the conductive trace and the conductive terminal; and

performing a solder reflow operation, thereby transforming a loose mechanical bond between the conductive trace and the substrate into a solid mechanical bond between the conductive trace and the substrate, wherein the interconnect reflows during the solder reflow operation and contacts and electrically connects the conductive trace and the conductive terminal after the solder reflow operation.

482. The method of claim 481, wherein forming the interconnect includes attaching a solder ball to the first contact terminal before aligning the substrate with the conductive trace and the chip.

483. The method of claim 481, including:

forming a first solder mask on the conductive trace, wherein the first solder mask includes a first opening;

forming a second solder mask on the substrate, wherein the second solder mask includes a second opening; then

aligning the substrate with the conductive trace and the chip such that the interconnect and the first and second openings are aligned with one another; and then

performing the solder reflow operation, wherein the interconnect extends into the first and second openings after the solder reflow operation.

484. The method of claim 483, including underfilling an adhesive that contacts and is sandwiched between the first and second solder masks after the solder reflow operation.

485. The method of claim 483, wherein the conductive trace provides horizontal routing for the pad within and outside the periphery of the chip, the conductive terminal provides horizontal and vertical routing for the pad outside the periphery of the chip, the connection joint provides vertical routing for the pad within the periphery of the chip, and the interconnect provides vertical routing for the pad outside the periphery of the chip.

486. A method of making a semiconductor chip assembly, comprising:

providing a semiconductor chip that includes first and second opposing major surfaces, wherein the first surface of the chip includes a conductive pad;

providing a conductive trace;

providing a substrate that includes first and second opposing major surfaces, wherein the first and second surfaces of the substrate include a conductive terminal and a dielectric base, the conductive terminal extends through the dielectric base and includes a first contact terminal at the first surface of the substrate and a second contact terminal at the second surface of the substrate, and a cavity extends from the first surface of the substrate into the substrate;

mechanically attaching the conductive trace to the chip using an adhesive;

forming an opening that extends through the adhesive and exposes the pad;

forming a connection joint in the opening that contacts and electrically connects the conductive trace and the pad; then

aligning the substrate with the conductive trace and the chip, wherein the first surfaces of the chip and the substrate face in a first direction, the second surfaces of the chip and the substrate face in a second direction, the chip extends into the cavity, the conductive trace is disposed within and outside a periphery of the chip and outside

the cavity, and an interconnect that includes solder is disposed between the conductive trace and the conductive terminal; and then

performing a solder reflow operation, thereby transforming a loose mechanical bond between the conductive trace and the substrate into a solid mechanical bond between the conductive trace and the substrate, wherein the interconnect reflows during the solder reflow operation and contacts and electrically connects the conductive trace and the conductive terminal after the solder reflow operation.

487. The method of claim 486, wherein forming the interconnect includes attaching a solder ball to the first contact terminal before aligning the substrate with the conductive trace and the chip.

488. The method of claim 486, including:

forming a first solder mask on the conductive trace, wherein the first solder mask includes a first opening;

forming a second solder mask on the substrate, wherein the second solder mask includes a second opening; then

aligning the substrate with the conductive trace and the chip such that the interconnect and the first and second openings are aligned with one another; and then

performing the solder reflow operation, wherein the interconnect extends into the first and second openings after the solder reflow operation.

489. The method of claim 488, including underfilling an adhesive that contacts and is sandwiched between the first and second solder masks after the solder reflow operation.

490. The method of claim 488, wherein the conductive trace provides horizontal routing for the pad within and outside the periphery of the chip, the conductive terminal provides horizontal and vertical routing for the pad outside the periphery of the chip, the connection joint provides vertical routing for the pad within the

periphery of the chip, and the interconnect provides vertical routing for the pad outside the periphery of the chip.

491. A method of making a semiconductor chip assembly, comprising:

providing a semiconductor chip that includes first and second opposing major surfaces, wherein the first surface of the chip includes a conductive pad;

providing a conductive trace;

providing a substrate that includes first and second opposing major surfaces, wherein the first and second surfaces of the substrate include a conductive terminal and a dielectric base, the conductive terminal extends through the dielectric base and includes a first contact terminal at the first surface of the substrate and a second contact terminal at the second surface of the substrate, and a cavity extends from the first surface of the substrate into the substrate;

aligning the chip with the conductive trace, wherein a connection joint that includes solder is disposed between the conductive trace and the pad;

aligning the substrate with the conductive trace and the chip, wherein the first surfaces of the chip and the substrate face in a first direction, the second surfaces of the chip and the substrate face in a second direction, the chip extends into the cavity, the conductive trace is disposed within and outside a periphery of the chip and outside the cavity, and an interconnect that includes solder is disposed between the conductive trace and the conductive terminal; and then

performing a solder reflow operation, thereby (i) transforming a loose mechanical bond between the conductive trace and the pad into a solid mechanical bond between the conductive trace and the pad, and (ii) transforming a loose mechanical bond between the conductive trace and the substrate into a solid mechanical bond between the conductive trace and the substrate, wherein the connection joint reflows during the solder reflow operation and contacts and electrically connects the conductive trace and the pad after the solder reflow operation, and the interconnect reflows during the solder reflow operation and contacts and electrically connects the conductive trace and the conductive terminal after the solder reflow operation.

492. The method of claim 491, wherein forming the connection joint includes attaching a solder bump to the pad before aligning the chip with the conductive trace, and forming the interconnect includes attaching a solder ball to the first contact terminal before aligning the substrate with the conductive trace and the chip.

493. The method of claim 491, including:

forming a first solder mask on the conductive trace, wherein the first solder mask includes a first inner opening and a first outer opening that are spaced and separated from one another;

forming a second solder mask on the substrate, wherein the second solder mask includes a second opening;

aligning the chip with the conductive trace such that the connection joint and the first inner opening are aligned with one another;

aligning the substrate with the conductive trace and the chip such that the interconnect and the first outer and second openings are aligned with one another; and then

performing the solder reflow operation, wherein the connection joint extends into the first inner opening and the interconnect extends into the first outer and second openings after the solder reflow operation.

494. The method of claim 493, including underfilling an adhesive that contacts and is sandwiched between the first and second solder masks after the solder reflow operation.

495. The method of claim 493, wherein the conductive trace provides horizontal routing for the pad within and outside the periphery of the chip, the conductive terminal provides horizontal and vertical routing for the pad outside the periphery of the chip, the connection joint provides vertical routing for the pad within the

periphery of the chip, and the interconnect provides vertical routing for the pad outside the periphery of the chip.

496. A method of making a semiconductor chip assembly, comprising:

providing a semiconductor chip that includes first and second opposing major surfaces, wherein the first surface of the chip includes a conductive pad;

providing a conductive trace;

providing a substrate that includes first and second opposing major surfaces, wherein the first and second surfaces of the substrate include a conductive terminal and a dielectric base, the conductive terminal extends through the dielectric base and includes a first contact terminal at the first surface of the substrate and a second contact terminal at the second surface of the substrate, and a cavity extends from the first surface of the substrate into the substrate;

aligning the chip with the conductive trace, wherein a connection joint that includes solder is disposed between the conductive trace and the pad; then

performing a first solder reflow operation, thereby transforming a loose mechanical bond between the conductive trace and the pad into a solid mechanical bond between the conductive trace and the pad, wherein the connection joint reflows during the first solder reflow operation and contacts and electrically connects the conductive trace and the pad after the first solder reflow operation; then

aligning the substrate with the conductive trace and the chip, wherein the first surfaces of the chip and the substrate face in a first direction, the second surfaces of the chip and the substrate face in a second direction, the chip extends into the cavity, the conductive trace is disposed within and outside a periphery of the chip and outside the cavity, and an interconnect that includes solder is disposed between the conductive trace and the conductive terminal; and then

performing a second solder reflow operation, thereby transforming a loose mechanical bond between the conductive trace and the substrate into a solid mechanical bond between the conductive trace and the substrate, wherein the interconnect reflows during the second solder reflow operation and contacts and

electrically connects the conductive trace and the conductive terminal after the second solder reflow operation.

497. The method of claim 496, wherein forming the connection joint includes attaching a solder bump to the pad before aligning the chip with the conductive trace, and forming the interconnect includes attaching a solder ball to the first contact terminal before aligning the substrate with the conductive trace and the chip.

498. The method of claim 496, including:

forming a first solder mask on the conductive trace, wherein the first solder mask includes a first inner opening and a first outer opening that are spaced and separated from one another;

forming a second solder mask on the substrate, wherein the second solder mask includes a second opening;

aligning the chip with the conductive trace such that the connection joint and the first inner opening are aligned with one another;

performing the first solder reflow operation, wherein the connection joint extends into the first inner opening after the first solder reflow operation; then

aligning the substrate with the conductive trace and the chip such that the interconnect and the first outer and second openings are aligned with one another; and then

performing the second solder reflow operation, wherein the interconnect extends into the first outer and second openings after the second solder reflow operation.

499. The method of claim 498, including underfilling an adhesive that contacts and is sandwiched between the first and second solder masks after the second solder reflow operation.

500. The method of claim 498, wherein the conductive trace provides horizontal routing for the pad within and outside the periphery of the chip, the

conductive terminal provides horizontal and vertical routing for the pad outside the periphery of the chip, the connection joint provides vertical routing for the pad within the periphery of the chip, and the interconnect provides vertical routing for the pad outside the periphery of the chip.